Integrated IF Transceiver for Broadband Wireless Applications

FEATURES

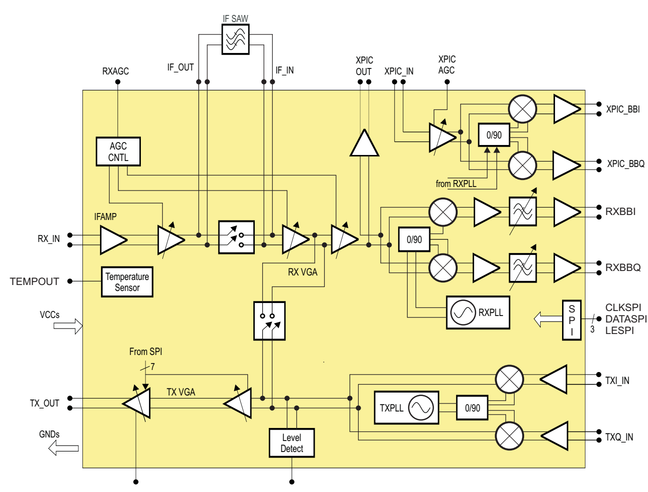
- **Integrated TX Chain (165–175 MHz / 330–350 MHz)**
  - **Baseband Amplifiers**
  - **Quadrature Modulator**
  - **Digitally Controlled VGA**
  - **TX Output IP3: 29.5 dBm**
  - **TX Output Noise: –166 dBc/Hz**
- **Integrated RX Chain (140–165 MHz / 280–330 MHz)**
  - **IF Amplifiers**
  - **Analog and Digital VGA**
  - **Quadrature Demodulator**
  - **Baseband Filters**
  - **ADC Buffers**
  - **IF SAW Filter Bypass**
  - **RX Noise Figure: 4.3 dB**
  - **RX Input IP3: 9.5 dBm**
- **Integrated TX and RX Synthesizers**
- **Integrated Cross-Polarization Interference Cancellation (XPIC) Support**
- **Auxiliary RX Chain**

APPLICATIONS

- **Wireless Microwave Backhaul**
- **Point-to-Point Microwave**
- **Broadband Wireless Applications**
- **WiMAX IF Transceiver**

DESCRIPTION

The TRF2443 is a highly integrated full-duplex intermediate frequency (IF) transceiver designed for broadband point-to-point wireless communications applications. The receiver chain integrates a quadrature (IQ) demodulator and provides more than 90 dB of gain range, obtained via a combination of analog- and digital-controlled VGAs. The integrated programmable baseband low-pass filter gives the TRF2443 the flexibility to receive signals with different bandwidths, while also helping to remove interferer signals before they reach the ADC. Additionally, the TRF2443 gives the flexibility to add an external IF filter to further remove unwanted signals. The TRF2443 transmitter chain integrates a quadrature (IQ) modulator driving a highly linear IF DVGA that provides 35 dB of gain range controlled via a serial programming interface (SPI). The TRF2443 includes the two synthesizers for the receiver and transmitter chains, removing the need for external LO generation circuitry and simplifying the implementation of a frequency-division duplexing (FDD) transceiver design. The TRF2443 also provides cross-polarization interference cancellation (XPIC) support via an integrated XPIC output amplifier and receiver chain. The TRF2443 is an ideal building block for implementing the IF transceiver function in the indoor unit (IDU), which is connected via a coaxial cable interface to the outdoor unit (ODU), of a point-to-point microwave backhaul split-architecture system.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TRF2443 DEVICE DESCRIPTION

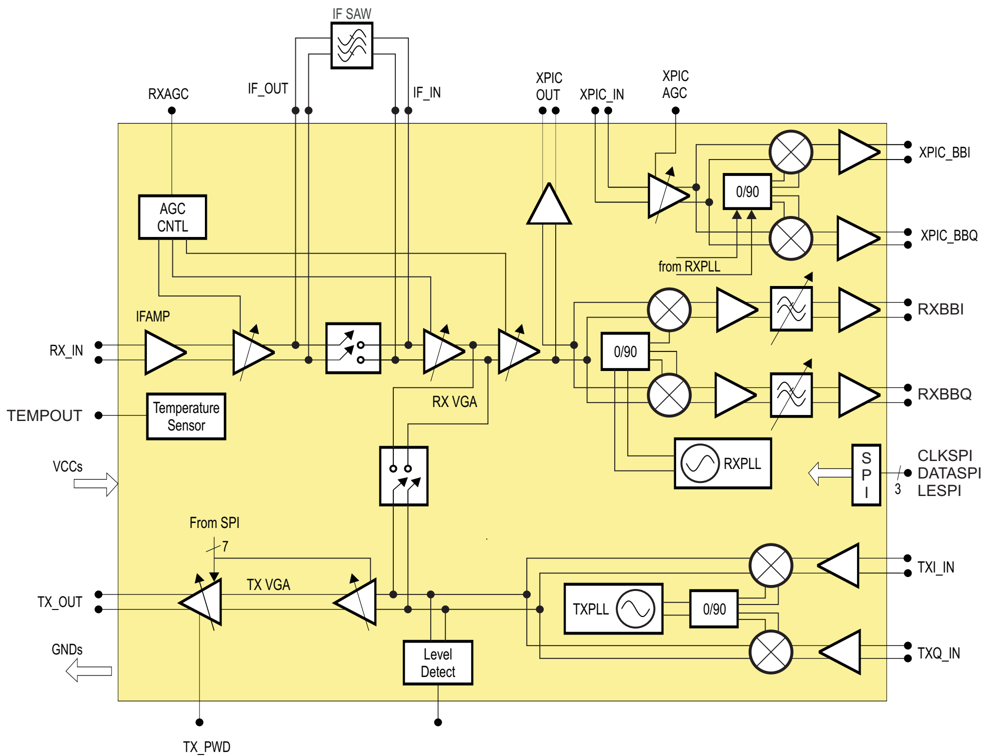


Figure 1. TRF2443 Functional Block Diagram

RECEIVER DESCRIPTION

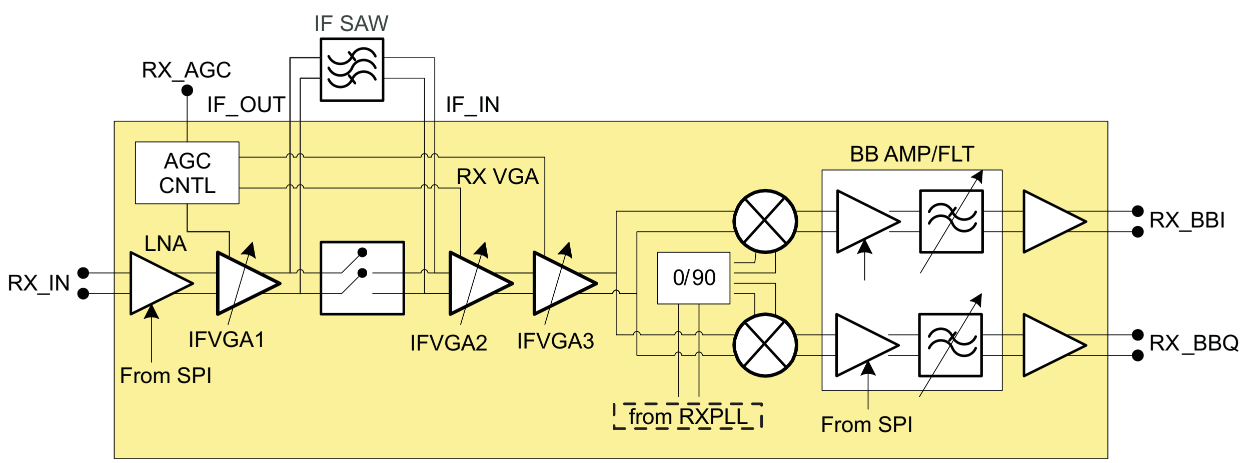


Figure 2. Receiver Chain Block Diagram

The TRF2443 features a highly linear low-noise receiver chain with over 60 dB of analog-controlled gain range and more than 40 dB of gain range programmable via the serial programming interface (SPI) in 1-dB steps. Moreover, the TRF2443 gives the flexibility to add an external IF filter to further remove unwanted signals. Such an external filter can be bypassed using an internal path that can be enabled via SPI. The first block of the receiver chain is a low-noise, highly linear IF amplifier (LNA). Its input is differential and internally matched to 50 Ω. The TRF2443 LNA attenuation is programmable from 0 dB to –19 dB, corresponding to an LNA gain of 17 dB to –2 dB (1-dB steps). The LNA is followed by three analog-controlled VGAs that provide more than 60 dB of gain range. The IFVGA1 output and IFVGA2 input can be connected externally (pins IFOUT and IFIN) through an external IF filter. An internal switch gives the flexibility to bypass the external filter. The VGAs provide a gain slope of 51 dB/V. The IFVGA3 drives the demodulator, which downconverts the IF input signal directly to baseband in-phase and quadrature. The demodulator block includes the local oscillator in-phase and quadrature generation circuitry followed by the LO buffer. The TRF2443 baseband section integrates a programmable-gain amplifier (PGA) and programmable low-pass filter. The baseband PGA minimum gain is 9 dB, and the maximum gain is 33 dB. The TRF2443 baseband low-pass filter cutoff frequency can be programmed from 2 MHz to 11 MHz by setting the cutoff-frequency control bits appropriately. The baseband output buffers (ADC drivers) are designed to drive directly an analog-to-digital converter (ADC), either dc- or ac-coupled. The output common mode of the ADC drivers is set externally via the RXBBCM pin (pin 40). When the TRF2443 is dc-connected to the ADC, the same dc common mode can be used for both the ADC and the TRF2443 baseband output.

TRANSMITTER DESCRIPTION

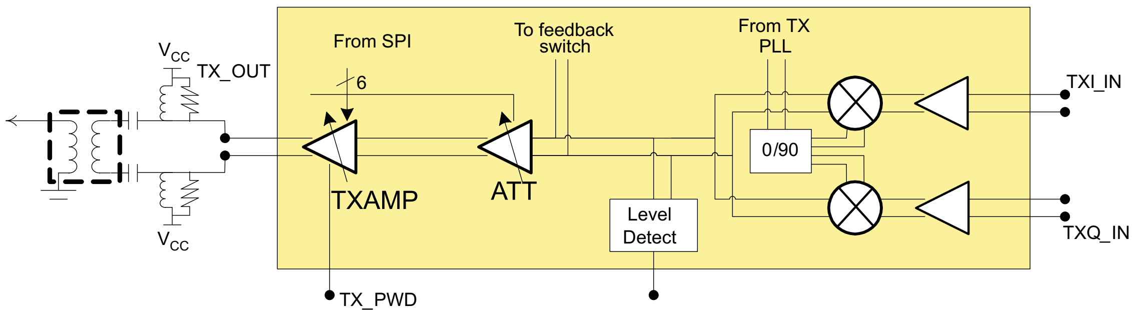


Figure 3. Transmitter Chain Block Diagram

The transmitter chain integrates an IQ modulator followed by a variable attenuator and the final transmitter amplification stage. The last two blocks provide over 35 dB of gain range. A power-alarm circuit monitors the level at the modulator output, and its digital output goes low if the signal level falls below the user-specified threshold level relative to the expected level. The first block of the transmitter chain is the IQ modulator, which upconverts the incoming in-phase and quadrature signals to the TX IF frequency. The TRF2443 can be either ac- or dc-coupled to the digital-to-analog converter (DAC). The IQ modulator drives a variable attenuator. This block provides 5.5 dB of total attenuation range in 0.5-dB steps. The output amplifier integrates five attenuation steps of 6 dB each for total of 30 dB. The output amplifier in combination with the variable attenuator provides over 35.5 dB of monotonic output power control (0.5-dB steps).

SYNTHESIZERS DESCRIPTION

TRF2443 integrates two complete integer synthesizers for the receiver and transmitter chain. The RXVCO operates at 16 times the typical RX input frequency, and the TXVCO operates at 8 times the typical TX output frequency.

Each synthesizer is composed of:

- High-frequency VCO (around 2720 MHz for the TX VCO and 2240 MHz for the RX VCO)
- N-divider (driven by the high-frequency VCO) done by an 8/9 prescaler followed by an A-B counter that drives the phase-frequency detector
- Phase-frequency detector (PFD) (driven by the N-divider) that compares the VCO divided by N to the reference clock divided by R signals
- Charge pump (driven by the PFD) which creates up and down current pulses, based on the incoming signals from the PFD. Its output is filtered and transformed to voltage by the external loop filter and applied to the VCO input control voltage.
- An external reference clock must be applied to the REFIN (pin 16). The incoming signal is buffered and goes through a programmable divider (R-divider).

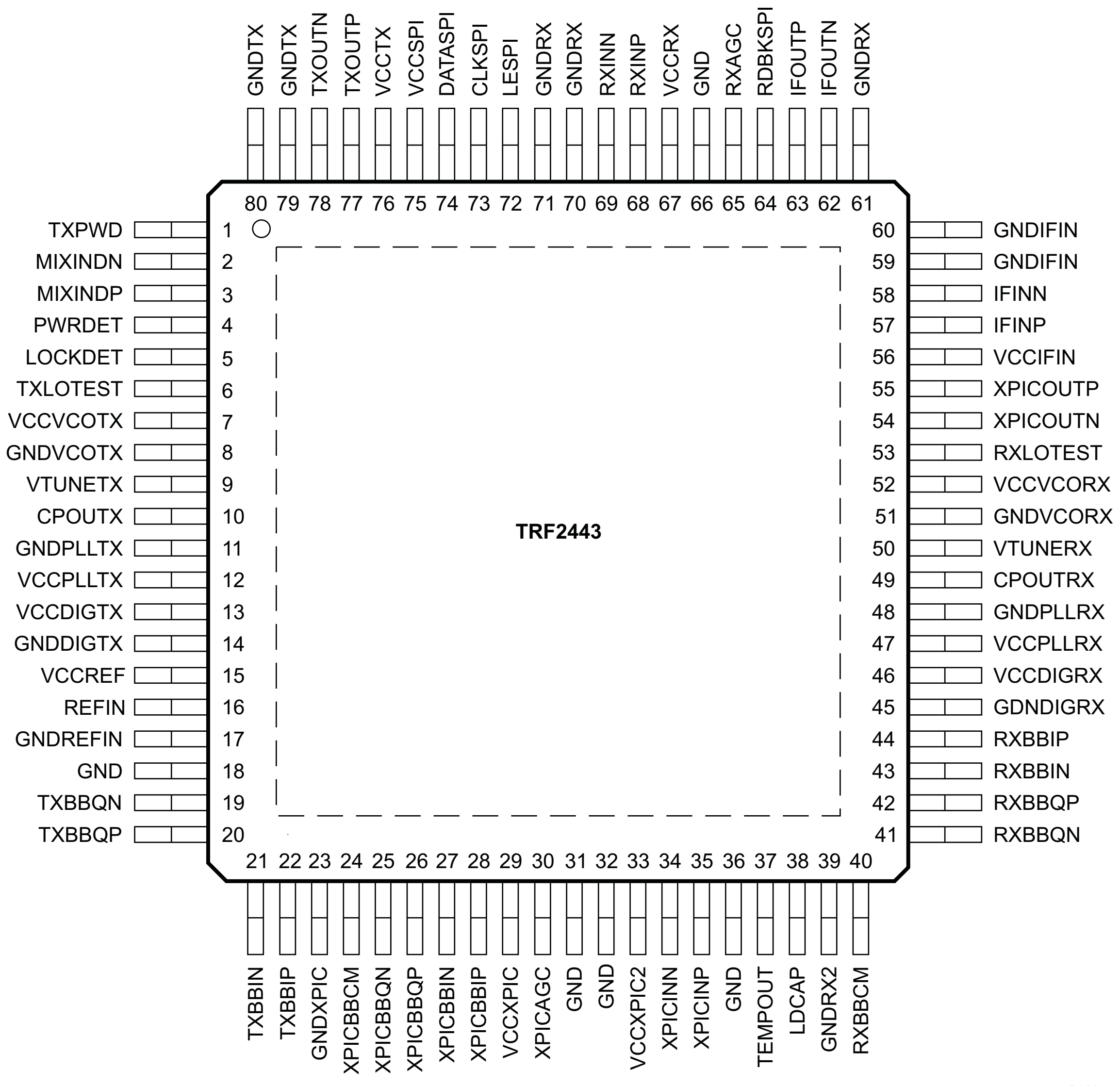
The VCO output is then routed through a programmable divider by 8 or 16 to create the TX and RX LO signals. The TRF2443 features a lock-detect output pin (LOCKDET, pin 5). This is a digital output that is high when both RX and TX synthesizers are locked, and it is low if one or both synthesizers are unlocked (or lose lock).

XPIC DESCRIPTION

The TRF2443 provides cross-polarization interference cancellation (XPIC) support via an integrated XPIC output amplifier and receiver chain. The XPIC output amplifier transmits the signal taken at the receiver demodulator input. The XPIC receiver section downconverts the input signal to baseband I and Q. It includes an IF VGA followed by a demodulator and a baseband amplifier.

PINOUT DIAGRAM

PFP Package
(Top View)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CLKSPI	73	I	SPI clock
CPOUTRX	49	O	RX PLL charge-pump output
CPOUTX	10	O	TX PLL charge-pump output
DATASPI	74	I	SPI data
GND	18, 31, 32, 36, 66	–	Ground
GNDDIGRX	45	–	RX PLL digital ground
GNDDIGTX	14	–	TX PLL digital ground
GNDIFIN	59, 60	–	RX chain ground
GNDPLLRX	48	–	RX PLL ground
GNDPLLTX	11	–	TX PLL ground
GNDREFIN	17	–	Reference clock ground
GNDRX	61, 70, 71	–	RX chain ground
GNDRX2	39	–	RX chain ground
GNDTX	79, 80	–	TX chain ground
GNDVCORX	51	–	RX VCO ground
GNDVCOTX	8	–	TX VCO ground
GNDXPIC	23	–	XPIC ground
IFINN	58	I	IFVGA2 input: negative terminal
IFINP	57	I	IFVGA2 input: positive terminal
IFOUTN	62	O	IFVGA1 output: negative terminal
IFOUTP	63	O	IFVGA1 output: positive terminal
LDCAP	38	I/O	PLL lock detector decoupling capacitor pin
LESPI	72	I	SPI latch enable
LOCKDET	5	O	PLL lock detect output (digital HIGH = locked, LOW = unlocked)
MIXINDN	2	O	TX mixer output collector: negative terminal
MIXINDP	3	O	TX mixer output collector: positive terminal
PWRDET	4	O	Power alarm output (digital HIGH = output power above threshold; LOW = output power below threshold)
RDBKSPI	64	O	SPI data readback
REFIN	16	I	PLL reference clock input
RXAGC	65	I	RX AGC control input
RXBBCM	40	I	RX chain common-mode input
RXBBIN	43	O	RX baseband output I: negative terminal
RXBBIP	44	O	RX baseband output I: positive terminal
RXBBQN	41	O	RX baseband output Q: negative terminal
RXBBQP	42	O	RX baseband output Q: positive terminal
RXINN	69	I	RX input: negative terminal
RXINP	68	I	RX input: positive terminal
RXLOTEST	53	O	RX LO test pin
TEMPOUT	37	O	Temperature sensor output
TXBBIN	21	I	TX baseband I input: negative input
TXBBIP	22	I	TX baseband I input: positive input
TXBBQN	19	I	TX baseband Q input: negative input
TXBBQP	20	I	TX baseband Q input: positive input

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TXLOTEST	6	O	TX LO test pin
TXOUTN	78	O	TX IF output: negative terminal
TXOUTP	77	O	TX IF output: positive terminal
TXPWD	1	I	TX power down
VCCDIGRX	46	–	RX PLL digital power supply
VCCDIGTX	13	–	TX PLL digital power supply
VCCIFIN	56	–	RX chain power supply
VCCPLLTX	12	–	TX PLL power supply
VCCPLLRX	47	–	RX PLL power supply
VCCREF	15	–	Reference clock power supply
VCCRX	67	–	RX chain power supply
VCCSPI	75	–	SPI power supply
VCCTX	76	–	TX power supply
VCCVCORX	52	–	RX VCO power supply
VCCVCOTX	7	–	TX VCO power supply
VCCXPIC	29	–	XPIC power supply
VCCXPIC2	33	–	XPIC power supply
VTUNERX	50	I	RX VCO input control voltage
VTUNETX	9	I	VCO tune voltage input
XPICAGC	30	I	XPIC AGC control input
XPICBBCM	24	I	XPIC common-mode input
XPICBBIN	27	O	XPIC baseband I output: negative terminal
XPICBBIP	28	O	XPIC baseband I output: positive terminal
XPICBBQN	25	O	XPIC baseband Q output: negative terminal
XPICBBQP	26	O	XPIC baseband Q output: positive terminal
XPICINN	34	I	XPIC input
XPICINP	35	I	XPIC input
XPICOUTN	54	O	XPIC output
XPICOUTP	55	O	XPIC output

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
	Input voltage range(2)	–0.3 to 5	V
	ESD rating, HBM	2000	V
	ESD rating, CDM	500	V
T_J	Junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL CHARACTERISTICS

Over recommended operating free-air temperature (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JA}	Thermal derating, junction-to-ambient	High-K board, still air		8.5		°C/W

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC_3V}	3.3-V power-supply voltage	3	3.3	3.6	V
V_RXAGC	Analog AGC voltage (pin 65)	0		2	V
V_XPICAGC	Analog AGC voltage (pin 30)	0		1	V
T_J	Operating junction temperature	0	65	125	°C
T_A	Operating ambient temperature	–40		85	°C

DC CHARACTERISTICS

V_{CC} = 3.3 V; T_J = 65°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Total supply current	TX on; RX on (SAW off); XPIC off		947		mA
		TX on; RX on (SAW on); XPIC off		965		
		TX on; RX on (SAW on); XPIC on		1085		

DIGITAL INTERFACE CHARACTERISTICS

V_{CC} = 3.3 V; T_J = 65°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage		0.8 V_{CC}			V
V_{OL}	Low-level output voltage				0.2 V_{CC}	V

RECEIVER CHARACTERISTICS

V_{CC_3V} = 3.3 V ±5%, T_J = 65°C , IF SAW filter insertion loss = 10 dB(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IF}	Input IF frequency			140		MHz
From RX_IN to RX_BBI/RX_ BBQ						
G_{max} (2)	Maximum voltage gain	LNA_ATT = 0; RXAGC = 2 V(3)	76	86		dB
		LNA_ATT = 0; RXAGC = 2 V(4)	69			
		LNA_ATT = 17; RXAGC = 2 V(3)	59	68		
		LNA_ATT = 17; RXAGC = 2 V(4)	52			
G_{min} (2)	Minimum voltage gain	LNA_ATT = 0; RXAGC = 0 V(3)		12	25	dB
		LNA_ATT = 0; RXAGC = 0 V(4)		12	27	
		LNA_ATT = 17; RXAGC = 0 V(3)			8	
		LNA_ATT = 17; RXAGC = 0 V(4)			10	
	LNA attenuation step	LNA_ATT = 17(5)	16.9	17.9	18.9	dB
ΔG_{step}	Digital gain step	LNA attenuation setting through SPI		1.05		dB
ΔG_{range}	Analog gain range	RXAGC from 0 V to 2 V(6)	54	62		dB
	Gain flatness	From 110 MHz to 170 MHz		1.5		dB
	Gain control slope			51		dB/V
NF	Noise figure(7)	LNA_ATT = 0(8)(9)		4.5	6	dB
		LNA_ATT = 17(10)(11)		18.5	23	
IP3	Input IP3	LNA_ATT = 0(12)(13)		-9.5		dBm
		LNA_ATT = 17(14)(15)	3	6.5		
Γin	Input return loss	Z_0 = 50 Ω, differential		–25	–12	dB
FROM RX_IN TO IF_OUT						
G_{max}	Maximum voltage gain			33		dB
ΔG_{dig}	Digital gain range	Programmed by SPI		20		dB
ΔG_{step}	Digital gain step			1.05		dB
ΔG_{analog}	Analog gain range			34		dB
NF	Noise figure	LNA_ATT = 0, RXAGC = 2 V		3.5		dB
		LNA_ATT = 17, RXAGC = 2 V		19.5		
IP3	Input IP3	LNA_ATT = 0, RXAGC = 2 V		–13		dBm
Γin	Input return loss	Z_0 = 50 Ω, differential			–12	dB

(1) 10 dB includes SAW filter insertion loss plus matching/board loss
(2) Gain measured from transformer input to RXBBI/Q output. External transformer insertion loss = 0.5 dB
(3) SAW filter path enabled; baseband amplifier gain setting set to 9
(4) SAW filter path disabled; baseband amplifier gain setting set to 0
(5) Attenuation measured from LNA_ATT = 0 state.
(6) Monotonicity of RX gain versus VAGC is specified up to the maximum voltage gain spec and not the maximum VAGC voltage.
(7) Automated test equipment 1-sigma measurement uncertainty of 0.15 dB.
(8) SAW filter path disabled; baseband amplifier gain setting set to 0; total gain = 55 dB (gain measured from transformer input to RXBBI/Q output; external transformer insertion loss = 0.5 dB)
(9) SAW filter path enabled; baseband amplifier gain setting set to 3; total gain = 66 dB (gain measured from transformer input to RXBBI/Q output; external transformer insertion loss = 0.5 dB)
(10) SAW filter path disabled; baseband amplifier gain setting set to 0; total gain = 38 dB (gain measured from transformer input to RXBBI/Q output; external transformer insertion loss = 0.5 dB)
(11) SAW filter path enabled; baseband amplifier gain setting set to 3; total gain = 49 dB (gain measured from transformer input to RXBBI/Q output; external transformer insertion loss = 0.5 dB)
(12) SAW filter path enabled; baseband amplifier gain setting set to 9; total gain = 33 dB (gain measured from transformer input to RXBBI/Q output; external transformer insertion loss = 0.5 dB)
(13) SAW filter path disabled; baseband amplifier gain setting set to 0; total gain = 35 dB (gain measured from transformer input to RXBBI/Q output; external transformer insertion loss = 0.5 dB)
(14) SAW filter path enabled; baseband amplifier gain setting set to 9; total gain = 16 dB (gain measured from transformer input to RXBBI/Q output; external transformer insertion loss = 0.5 dB)
(15) SAW filter path disabled; baseband amplifier gain setting set to 0; total gain = 18 dB (gain measured from transformer input to RXBBI/Q output; external transformer insertion loss = 0.5 dB)

RECEIVER CHARACTERISTICS (continued)

V_{CC_3V} = 3.3 V ±5%, T_J = 65°C , IF SAW filter insertion loss = 10 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FROM IF_IN TO RX_BBI (OR RX_BBQ)						
G_{max}	Maximum voltage gain	RXAGC = 2 V, RXBB_GAIN = 9		58		dB
ΔG_{dig}	Digital gain range	Programmed by SPI		24		dB
ΔG_{step}	Digital gain step			1		dB
ΔG_{analog}	Analog gain range			28		dB
NF	Noise figure	RXAGC = 2 V, RXBB_GAIN = 9		12.5		dB
		RXAGC = 0 V, RXBB_GAIN = 9		28		
	Image rejection	See *RX Image Rejection* section		-40		dB
	Output common mode			1.5		V
	Baseband output load	Parallel capacitor		15		pF
		Parallel resistor		1		kΩ
BASEBAND LOW-PASS FILTER						
f_{C_ON}	3-dB cutoff frequency	Filter on, programmed via SPI	2		11	MHz
ATT_{30M}	Filter rejection at 30 MHz	Filter bypassed		1		dB
	Filter rejection	3-dB point with f_C = 2.3 MHz (16)	2.2			MHz
		3-dB corner-frequency step (17)		25		kHz
		Rejection at 4.5 MHz with f_C = 2.3 MHz (16)	36			dB
		Rejection at 8.75 MHz with f_C = 2.3 MHz (16)		76		
		Rejection at 17.5 MHz with f_C = 2.3 MHz (16)		80		
		3-dB point with f_C = 8.5 MHz (16)	8.3			MHz
		Rejection at 18 MHz with f_C = 8.5 MHz (16)	30			dB
		Rejection at 35 MHz with f_C = 8.5 MHz (16)	65			
		Rejection at 70 MHz with f_C = 8.5 MHz (16)		80		

(16) After room-temperature cutoff-frequency calibration
(17) Baseband filter 3-dB corner frequency control step via SPI around f_C = 2.3 MHz

TRANSMITTER CHARACTERISTICS

V_{CC_3V} = 3.3 V ± 5%, T_J = 65°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{lout}	TX output frequency			340		MHz
FROM TXBBI/Q INPUTS TO TX RFOUT						
P_{max}	Maximum output power	TX ATT set to 0 [1]	2.5			dBm
P_{min}	Minimum output power	TX ATT set to 35			–28.5	dBm
G_{range}	Gain range	Programmed by SPI	31			dB
G_{step}	1-dB gain step	Two consecutive 1-dB steps	0.8		1.2	dB
N_{out}	Output noise floor	TX ATT set to 4 [2]		–139	–135	dBm/Hz
		TX ATT set to 31 [2]		–166	–162	
OIP3	Output IP3	Two tones of –2.5 dBm each at TX output [3]	27.5	29.5		dBm
		Two tones of –29.5 dBm each at TX output [3]	0.5			
CS	Carrier leakage	Calibrated; TX ATT set to 4 [4]		–55	–35	dBm
SBS	Side-band suppression	Uncalibrated [5]		–50	–35	dB
HD2	Second harmonic level	See [1]		–55		dBc
HD3	Third harmonic level	See [1]		–50		dBc
τoff	TX turnoff time [6]	TX_PWD: low → high;	10		100	µs
	TX off attenuation [7]	TX_PWD = high	30			dB
VCM	Baseband input common-mode voltage [8]			1.4		V
Z_{BBin}	TX differential input impedance	Parallel resistor		10		kΩ
		Parallel capacitor		0.1		pF
Γout	Output return loss	Z_0 = 50 Ω [9]			–12	dB
POWER ALARM DETECTOR (See the *Power Alarm Detector* section)						
	Detector threshold	See [10]		See [11]	See [11]	dB
	Response time [12] (specified by design)		See [11]			µs

(1) Measured after the transformer (0.7-dB insertion loss) and with a TXBBI (or TXBBQ) input level of –23 dBVrms
(2) No signal applied to TRF2443. This parameter is assured by characterization and is not production tested.
(3) Two tones of –26 dBVrms each at TXBBI and TXBBQ inputs at 5 MHz and 8 MHz; measured at transformer output (0.7-dB insertion loss).
(4) Using internal common and dc offset control
(5) TXIQ_PHASE set to 8; SPI-3, register 1, B<17,13>
(6) See the *TX Output Power Ramp-Down* section.
(7) Attenuation of output level from TX on.
(8) Common mode input is set internally. It is possible to disable internal bias through SPI and apply external common mode.
(9) Single-ended, measured at transformer output
(10) Delta output power level at TX fixed gain that forces detector output low (power alarm).
(11) Detector threshold and response time are fully programmable by the user. (See the *Power Alarm Detector* section.)
(12) If output power is lower than threshold for more than user-specified value, power-alarm detector output goes low.

RF SYNTHESIZER CHARACTERISTICS

V_{CC_3V} = 3.3 V ±5%, T_J = 65°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TXVCO						
f_{txvco}	TXVCO frequency range	See (1)	2640		2800	MHz
f_{txlo}	TXLO frequency range	Divide-by-8 mode	330		350	MHz
		Divide-by-16 mode	165		175	
	TXLO free-running phase noise	f_{out} = 340 MHz; offset = 10 kHz		–92.5		dBc/Hz
		f_{out} = 340 MHz; offset = 100 kHz		–117.5		
		f_{out} = 340 MHz; offset = 1 MHz		–140		
		f_{out} = 340 MHz; offset = 20 MHz		–150		
Kv_{TX}	TXVCO gain			45		MHz/V
TXPLL						
f_{PFD}	PFD frequency			20		MHz
	TXLO closed-loop phase noise	f_{out} = 340 MHz; offset = 20 kHz		–117		dBc/Hz
		f_{out} = 340 MHz; offset = 100 kHz		–116		
		f_{out} = 340 MHz; offset = 1 MHz		–140		
		f_{out} = 340 MHz; offset = 20 MHz		–150		
	Integrated TXLO noise	Integrated from 1 kHz to 12 MHz; f_{out} = 340 MHz (2)		–56.5		dB
	Reference spur	Measured at TXLOTEST (2720 MHz)			–70	dBc
	Lock time	From unlocked state to locked state (includes digital-calibration time) (3)		300		µs
	TXLO closed-loop phase noise	f_{out} = 165 MHz; offset = 20 kHz		–121		dBc/Hz
		f_{out} = 165 MHz; offset = 100 kHz		–120		
		f_{out} = 165 MHz; offset = 1 MHz		–141		
		f_{out} = 165 MHz; offset = 20 MHz		–147		
Vcc_{min}	PLL-lock minimum power supply	T_J = 65°C	2.8			V
RXVCO						
f_{rxvco}	RXVCO frequency range	See (1)	2240		2640	MHz
f_{rxlo}	RXLO frequency range	Divide-by-8 mode	280		330	MHz
		Divide-by-16 mode	140		165	
	RXLO free-running phase noise	f_{out} = 140 MHz; offset = 10 kHz		–97.5		dBc/Hz
		f_{out} = 140 MHz; offset = 100 kHz		–122.5		
		f_{out} = 140 MHz; offset = 1 MHz		–146		
		f_{out} = 140 MHz; offset = 20 MHz		–150		
Kv_{RX}	RXVCO gain			45		MHz/V
RXPLL						
f_{PFD}	PFD frequency			20		MHz
	Integrated RXLO noise	Integrated from 1 kHz to 12 MHz; f_{out} = 140 MHz (2)		–62		dB
		Integrated from 1 kHz to 12 MHz; f_{out} = 160 MHz (2)		–60		
	RXLO closed-loop phase noise	f_{out} = 140 MHz; offset = 20 kHz		–122		dBc/Hz
		f_{out} = 140 MHz; offset = 100 kHz		–121		
		f_{out} = 140 MHz; offset = 1 MHz		–146		
		f_{out} = 140 MHz; offset = 20 MHz		–150		
	Reference spur	Measured at RXLOTEST (2240 MHz)			–65	dBc
	Lock time	From unlock state to lock state (includes digital-calibration time) (3)		300		µs

(1) Frequency range proven locked with PFD frequency = 20 MHz
(2) Optimized for lowest integrated noise; see the *Reference-Clock Characteristics* table for recommended reference clock performance.
(3) Charge-pump current = 1 mA, PFD frequency = 20 MHz, loop filter optimized (see *Application Schematic* section)

REFERENCE-CLOCK CHARACTERISTICS

V_{CC} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ref}	Reference frequency			20		MHz
	Phase noise	1 kHz		–135		dBc/Hz
		Floor		–160		
	Reference-clock input level	REFIN pin, ac-coupled on board (internally dc-coupled)	0.8	2	3	V_{PP}

XPIC CHARACTERISTICS

V_{CC_3V} = 3.3 V ± 5%, T_J = 65°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
From RX_IN to XPIC_OUT						
f_{in}	Input frequency			140		MHz
P_{out}	Output power	P_{in} = –32 dBm, LNA ATT set to 0 (1)	–14	–12	–10	dBm
	Output power flatness	From 110 MHz to 170 MHz		1		dB
NF	Noise figure	LNA ATT set to 0, total gain = 20 dB		15	22	dB
OIP3	Output IP3	Two tones of –16 dBm each at 136 MHz and 144 MHz (1) (2) (3)	11.5	13		dBm
Γout	Output return loss	Z_0 = 75 Ω, single-ended			–12	dB
FROM XPIC_IN TO XPIC_BBI/Q						
G_{MAX}	Maximum gain (4)	XPIC_AGC = 0.7 V and XPICBB_GAIN set to 2	21	27		dB
G_{MIN}	Minimum gain (4)	XPIC_AGC = 0 V and XPICBB_GAIN set to 2		5	10	dB
	Gain control slope			46		dB/V
G_{DRange}	Digital gain range	Programmed via SPI		11		dB
	Gain flatness	Measured over 110 MHz to 170 MHz		1		dB
NF	Noise figure	XPICBB_GAIN set to 2; total gain = 21 dB		22	25	dB
IP3	Input IP3	XPICBB_GAIN set to 2; total gain = 21 dB	–4	0		dBm
		XPICBB_GAIN set to 2; total gain = 10 dB	6	9.5		
	Image rejection	See *RX Image Rejection* section		–40		dB
Γin	Input return loss	Z_0 = 75 Ω, single-ended			–12	dB
	Output common mode			1.5		V
	Baseband output load	Parallel capacitor		15		pF
		Parallel resistor		1		kΩ

(1) RXAGC voltage to have RXBBI (or RXBBQ) output level = –17 dBVrms
(2) LNA ATT set to 0; total power gain = 20 dB
(3) Measured at XPIC_OUT balun output (75-Ω characteristic impedance)
(4) Measured from differential output (XPICBBIP/N or XPICBBQP/N) to XPICINN input balun

RECEIVER TYPICAL CHARACTERISTICS

f_{in}= 140 MHz, SAW_EN = 0, LNA_ATT = 0, baseband gain setting = 0, 3-dB pad enabled (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

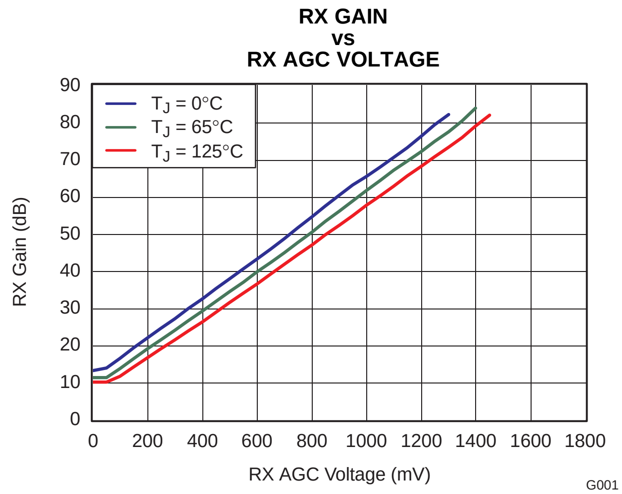


Figure 4.

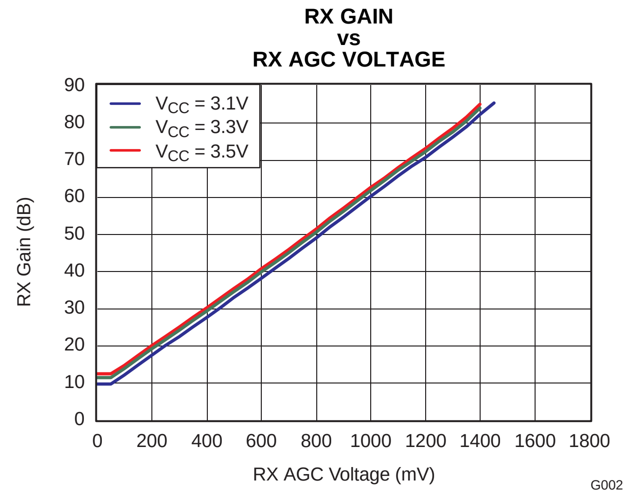


Figure 5.

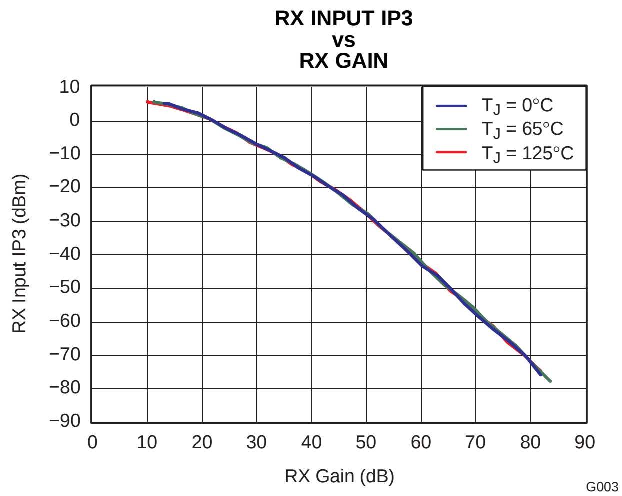


Figure 6.

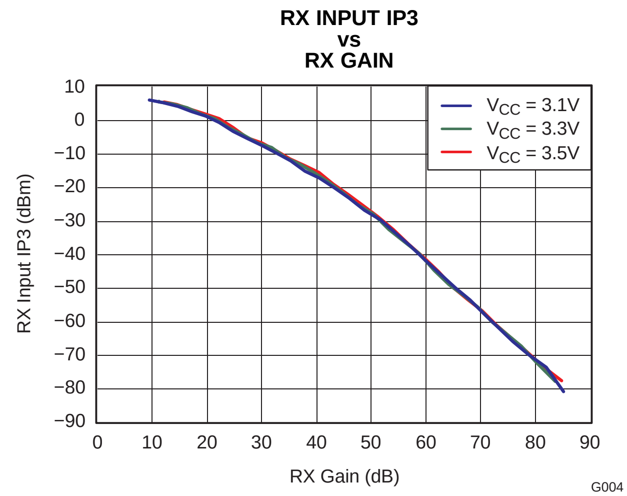


Figure 7.

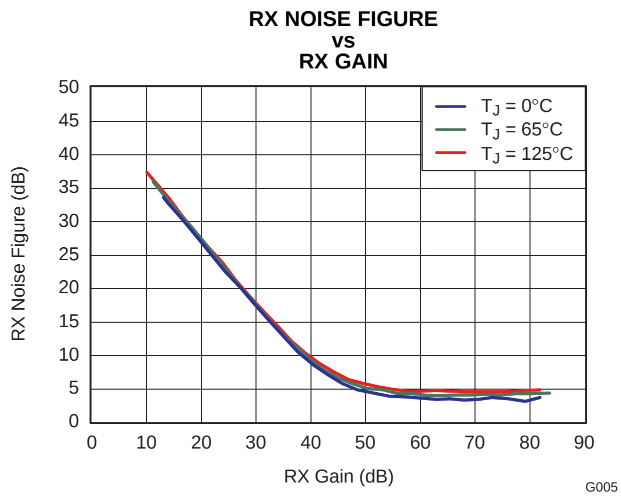


Figure 8.

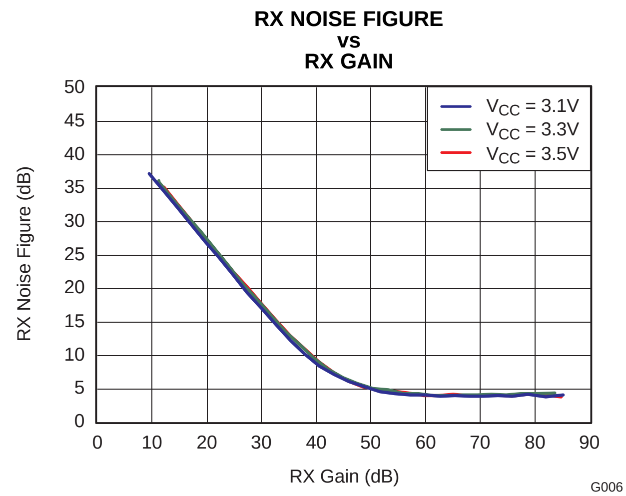


Figure 9.

RECEIVER TYPICAL CHARACTERISTICS

f_{in}= 140 MHz, SAW_EN = 1, LNA_ATT = 0, baseband gain setting = 3, 3-dB pad disabled (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

RX GAIN vs RX AGC VOLTAGE

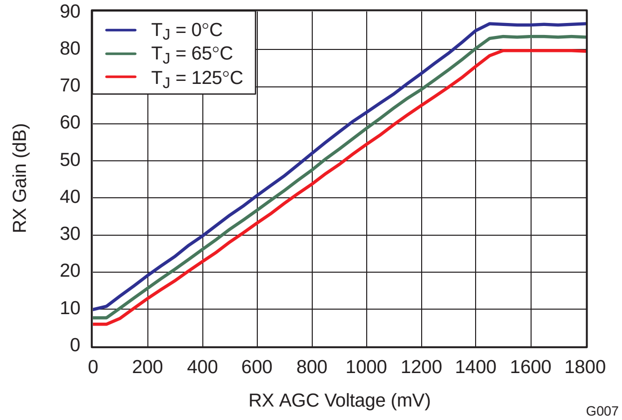


Figure 10.

RX GAIN vs RX AGC VOLTAGE

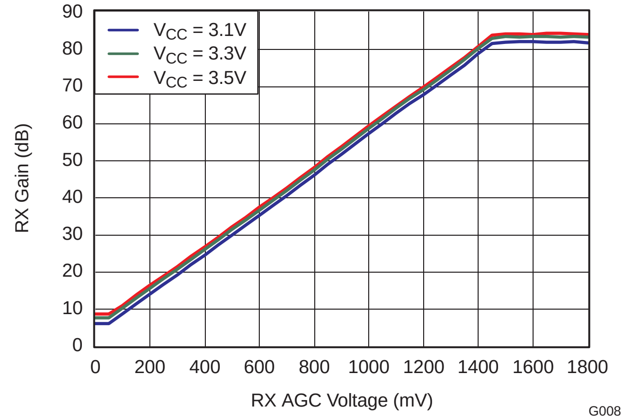


Figure 11.

RX INPUT IP3 vs RX GAIN

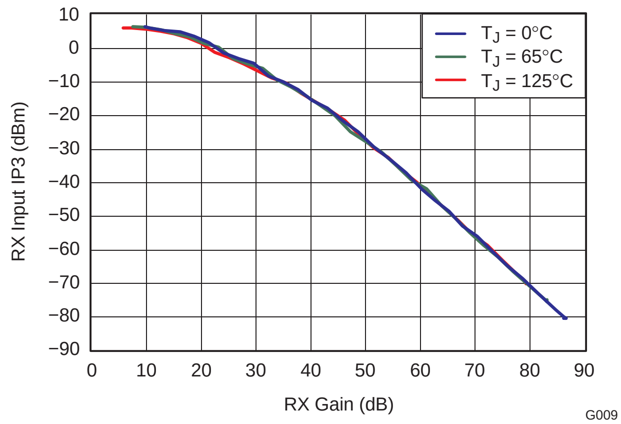


Figure 12.

RX INPUT IP3 vs RX GAIN

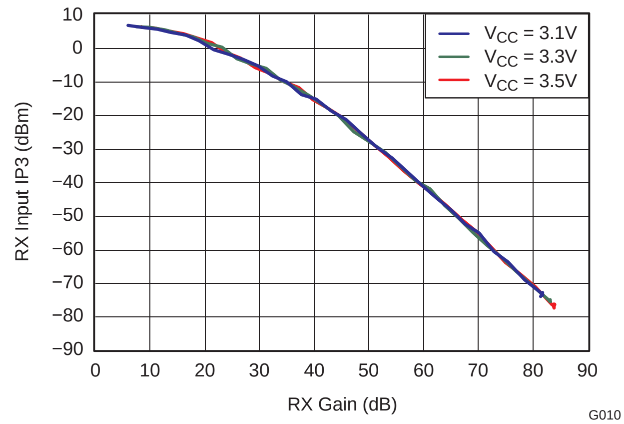


Figure 13.

RX NOISE FIGURE vs RX GAIN

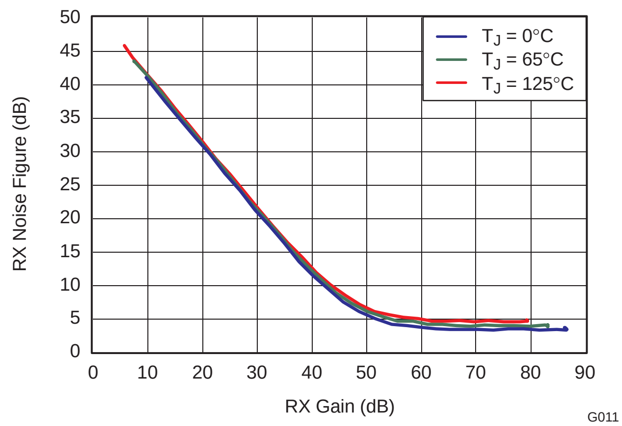


Figure 14.

RX NOISE FIGURE vs RX GAIN

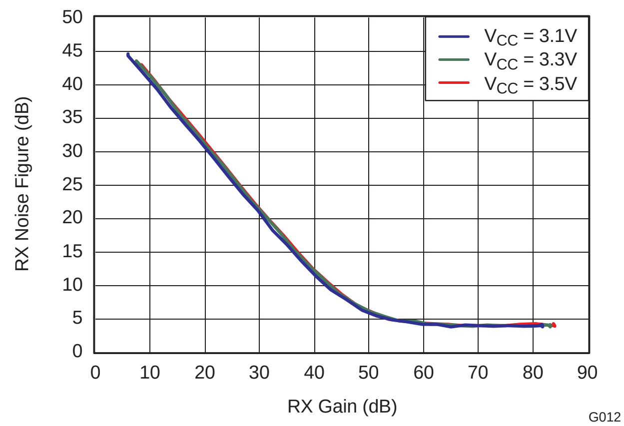


Figure 15.

RECEIVER TYPICAL CHARACTERISTICS

f_{in}= 140 MHz, SAW_EN = 1, LNA_ATT = 0, baseband gain setting = 6, 3-dB pad disabled (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

RX GAIN
vs
RX AGC VOLTAGE

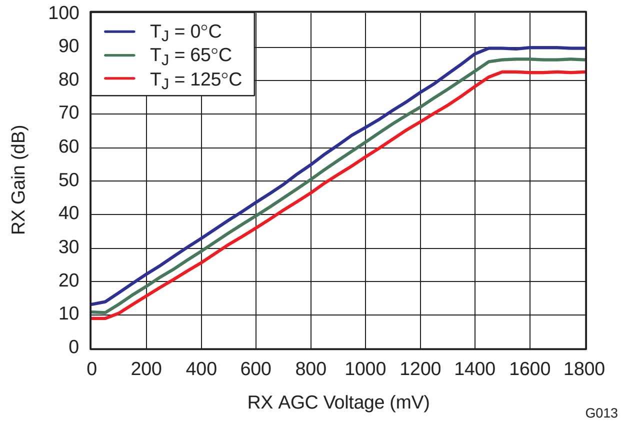


Figure 16.

RX GAIN
vs
RX AGC VOLTAGE

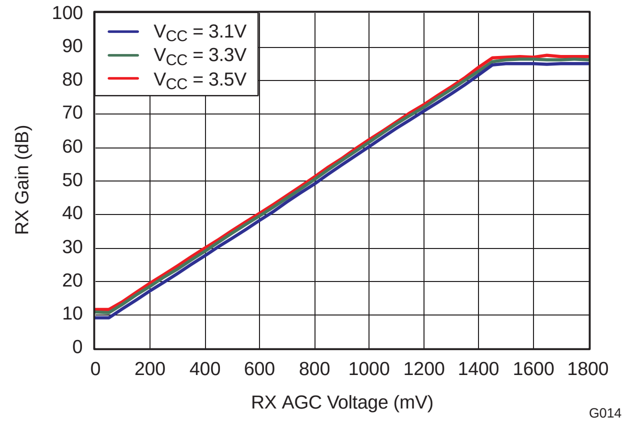


Figure 17.

RX INPUT IP3
vs
RX GAIN

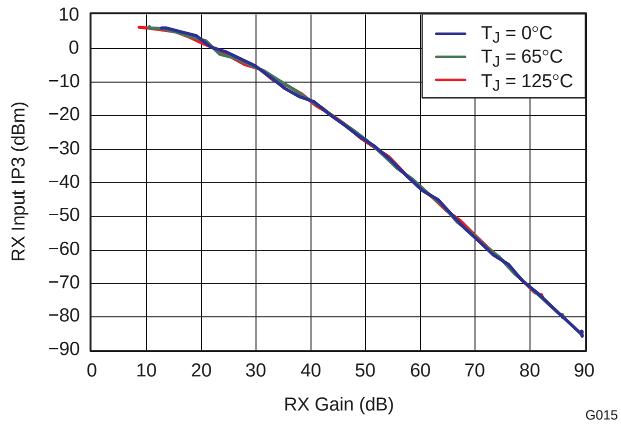


Figure 18.

RX INPUT IP3
vs
RX GAIN

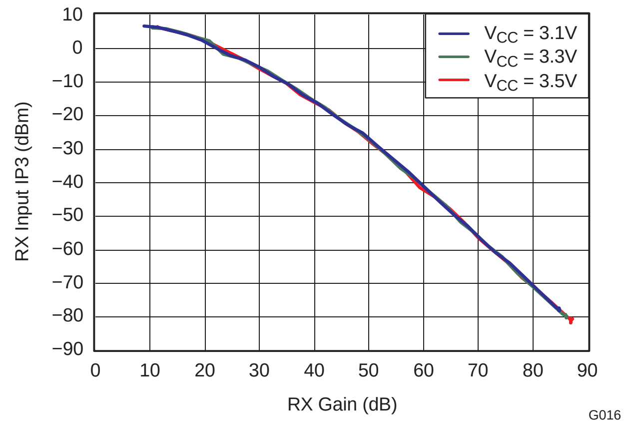


Figure 19.

RX NOISE FIGURE
vs
RX GAIN

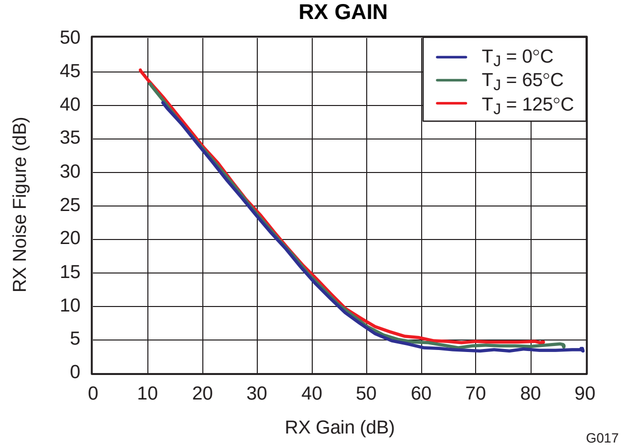


Figure 20.

RX NOISE FIGURE
vs
RX GAIN

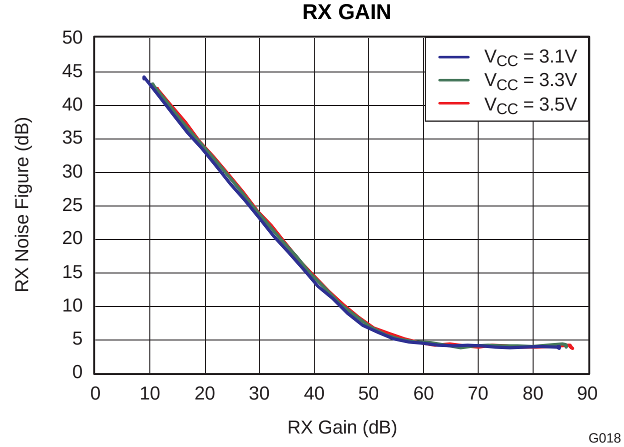


Figure 21.

RECEIVER TYPICAL CHARACTERISTICS

f_{in}= 140 MHz, SAW_EN = 1, LNA_ATT = 0, baseband gain setting = 9, 3-dB pad disabled (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

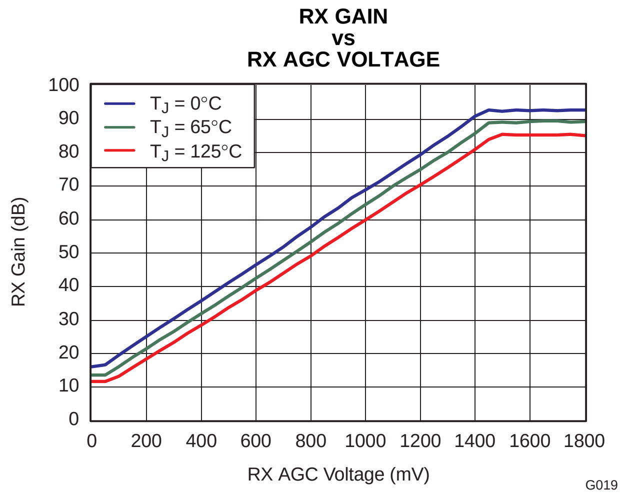


Figure 22.

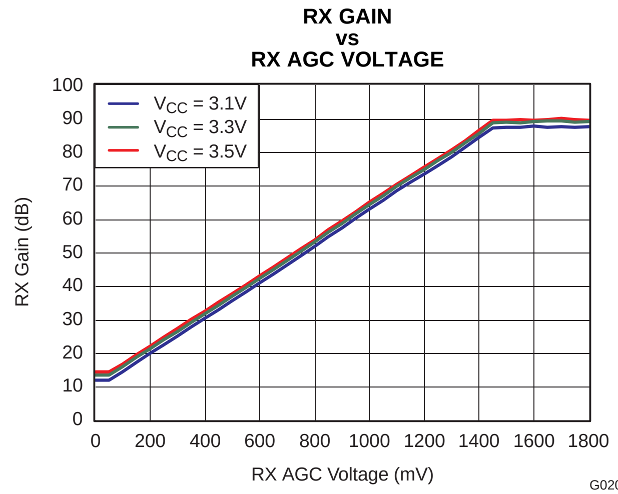


Figure 23.

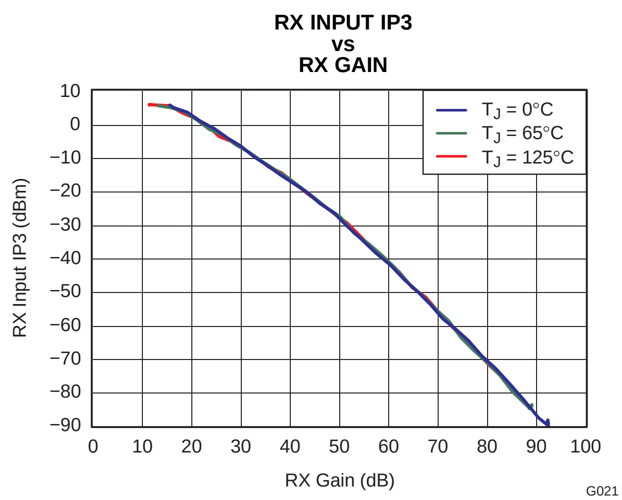


Figure 24.

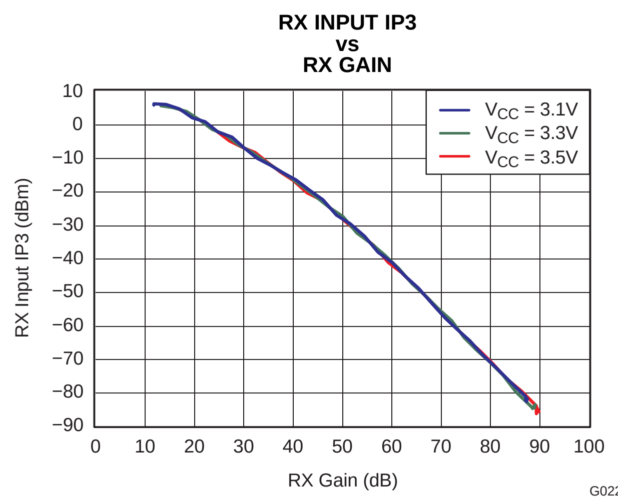


Figure 25.

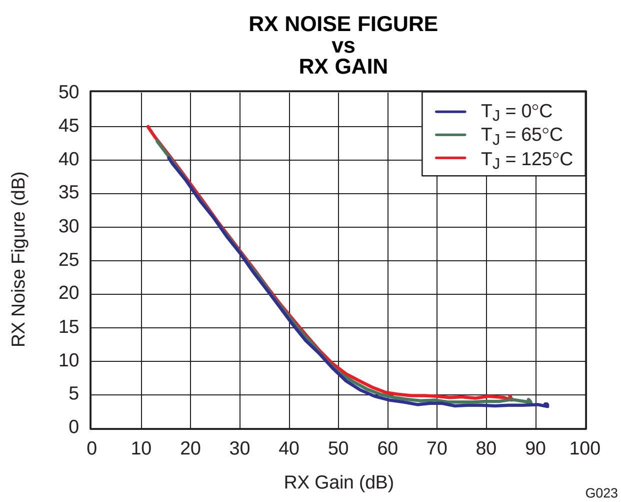


Figure 26.

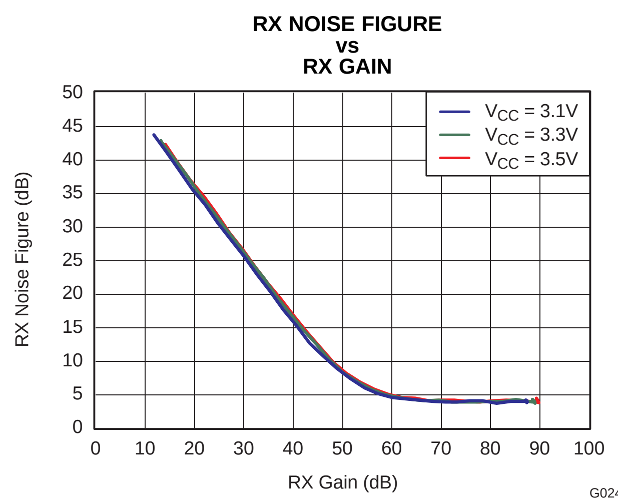


Figure 27.

RECEIVER TYPICAL CHARACTERISTICS

f_{in}= 140 MHz (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

RX LNA ATTENUATION vs LNA ATTENUATION SETTING

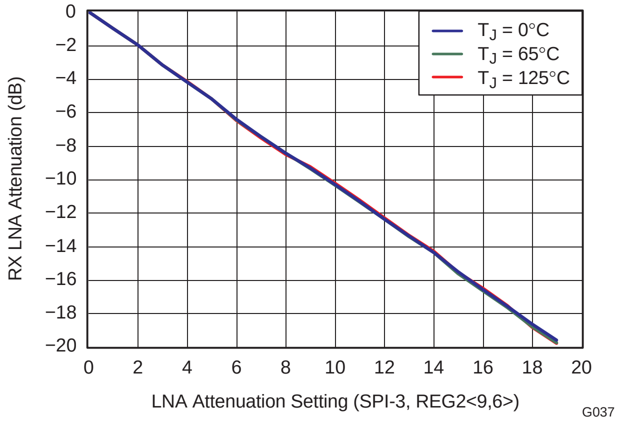


Figure 28.

RX LNA ATTENUATION vs LNA ATTENUATION SETTING

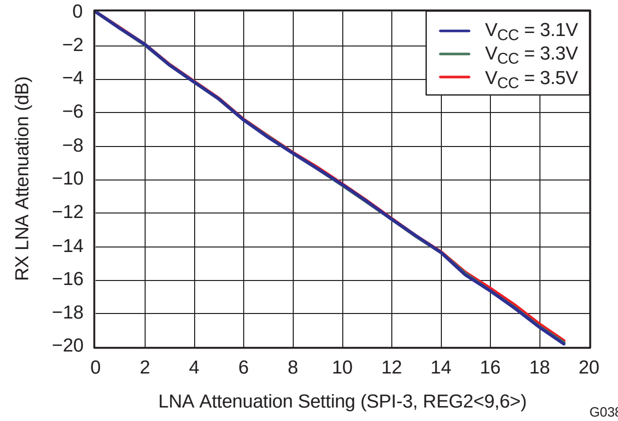


Figure 29.

RX LNA CUMULATIVE ATTENUATION ERROR vs LNA ATTENUATION SETTING

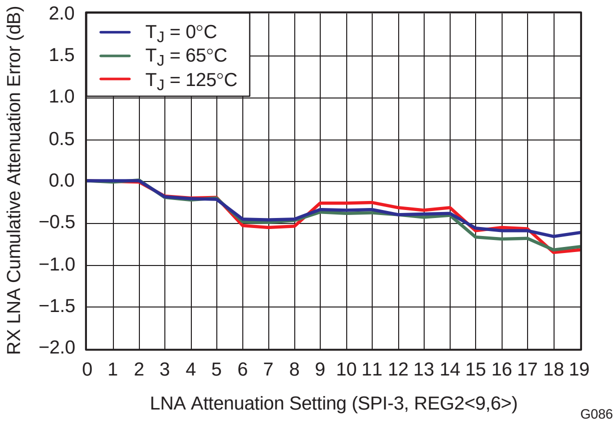


Figure 30.

RX LNA CUMULATIVE ATTENUATION ERROR vs LNA ATTENUATION SETTING

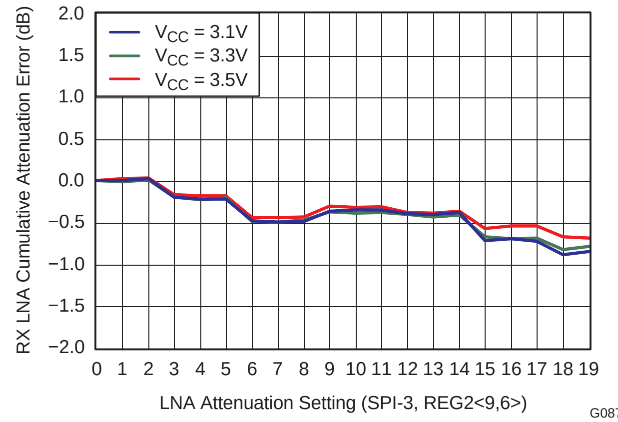


Figure 31.

RX BASEBAND GAIN vs RXBB GAIN SETTING

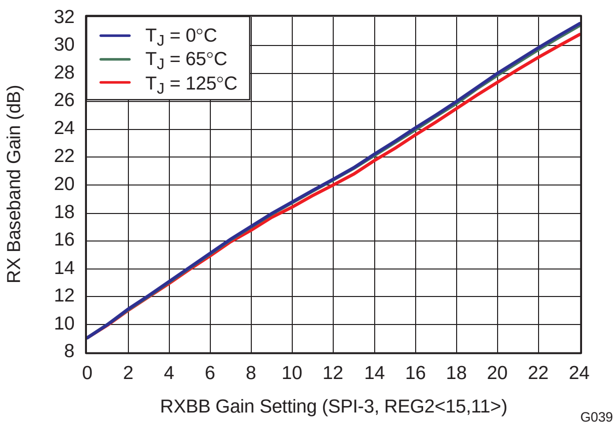


Figure 32.

RX BASEBAND GAIN vs RXBB GAIN SETTING

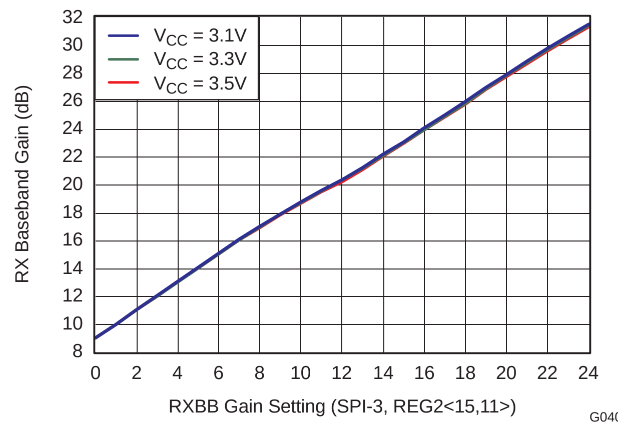


Figure 33.

RECEIVER TYPICAL CHARACTERISTICS (continued)

f_{in}= 140 MHz (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

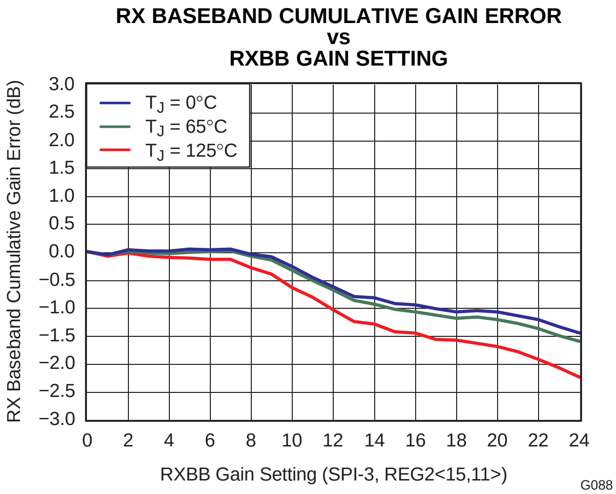


Figure 34.

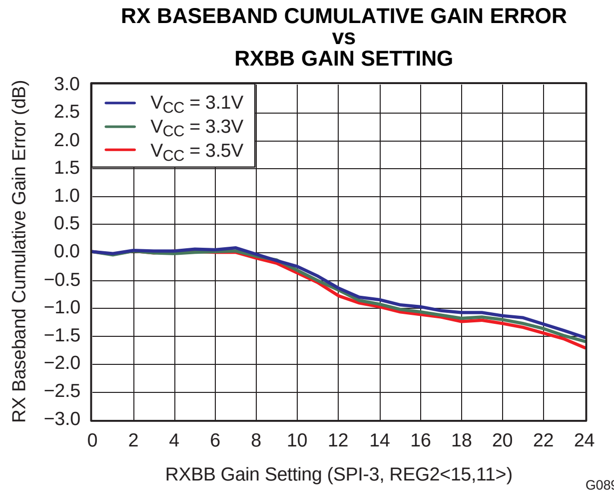


Figure 35.

RECEIVER TYPICAL CHARACTERISTICS

f_{in}= 280 MHz, SAW_EN = 0, LNA_ATT = 0, baseband gain setting = 0, 3-dB pad enabled (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

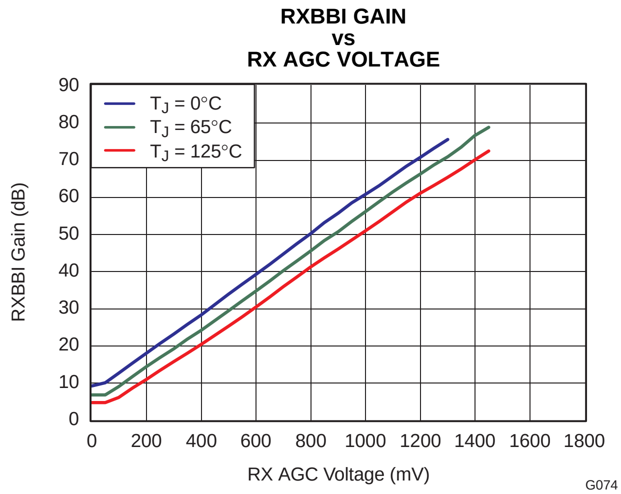


Figure 36.

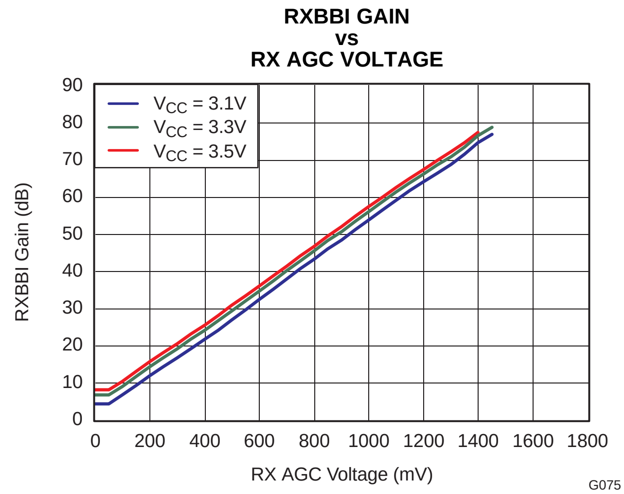


Figure 37.

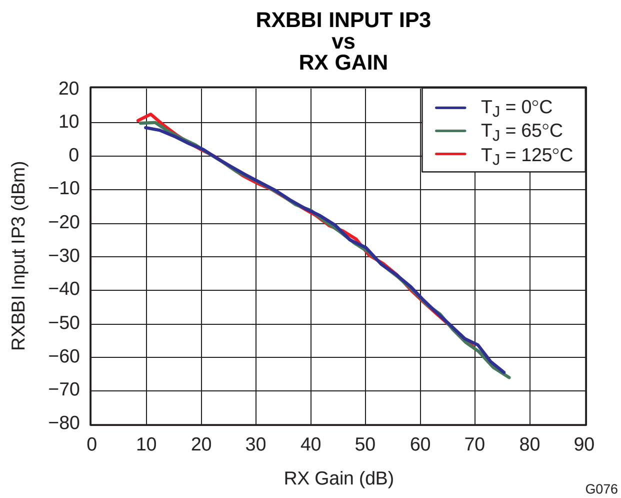


Figure 38.

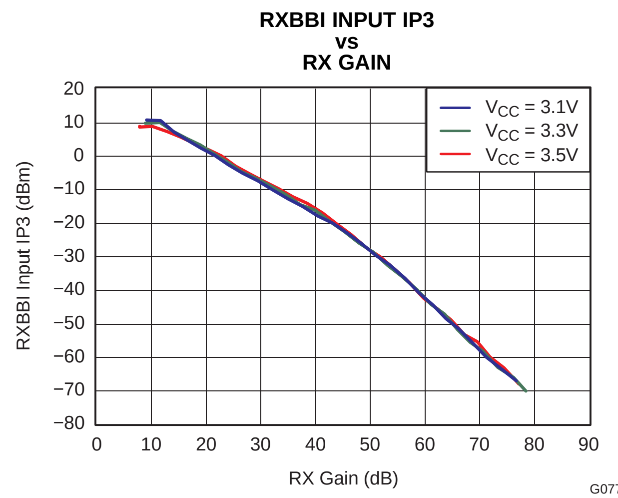


Figure 39.

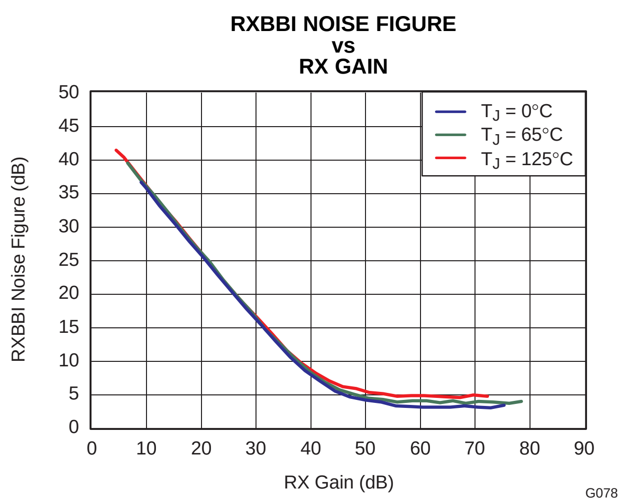


Figure 40.

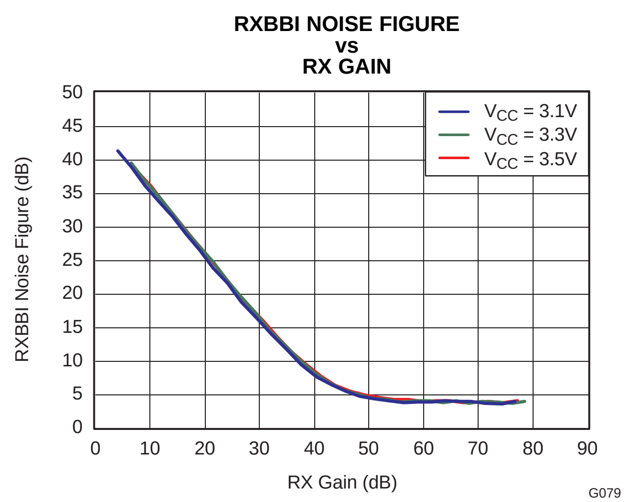


Figure 41.

RECEIVER TYPICAL CHARACTERISTICS

f_{in}= 280 MHz, SAW_EN = 1, LNA_ATT = 0, baseband gain setting = 9, 3-dB pad disabled (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

RXBBI GAIN vs RX AGC VOLTAGE

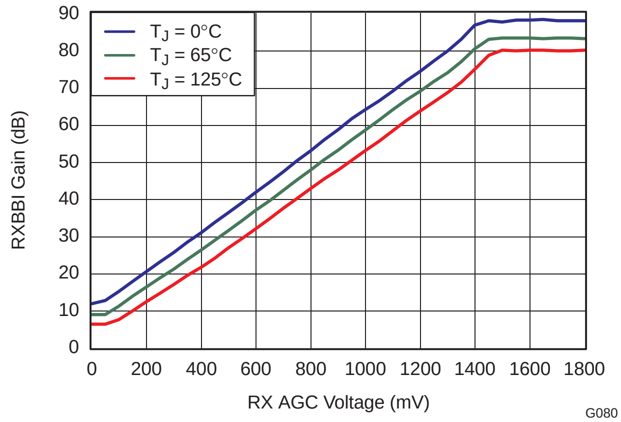


Figure 42.

RXBBI GAIN vs RX AGC VOLTAGE

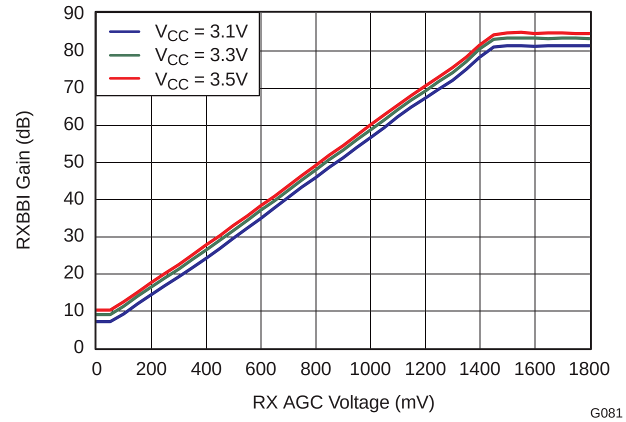


Figure 43.

RXBBI INPUT IP3 vs RX GAIN

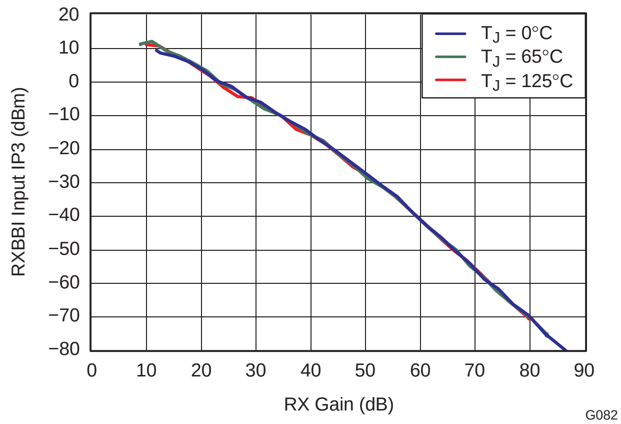


Figure 44.

RXBBI INPUT IP3 vs RX GAIN

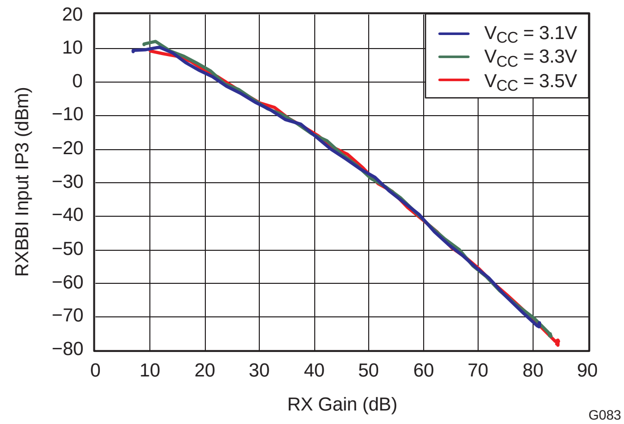


Figure 45.

RXBBI NOISE FIGURE vs RX GAIN

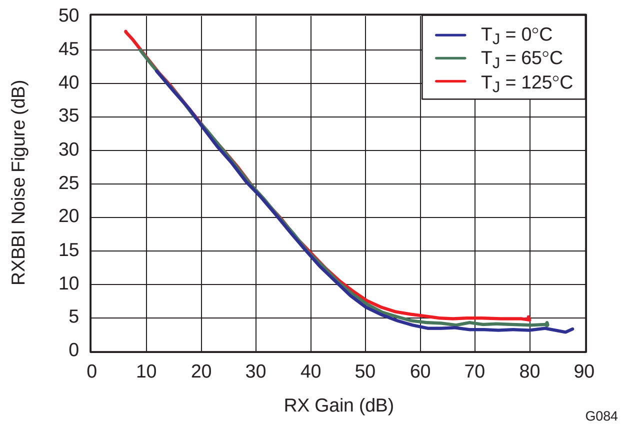


Figure 46.

RXBBI NOISE FIGURE vs RX GAIN

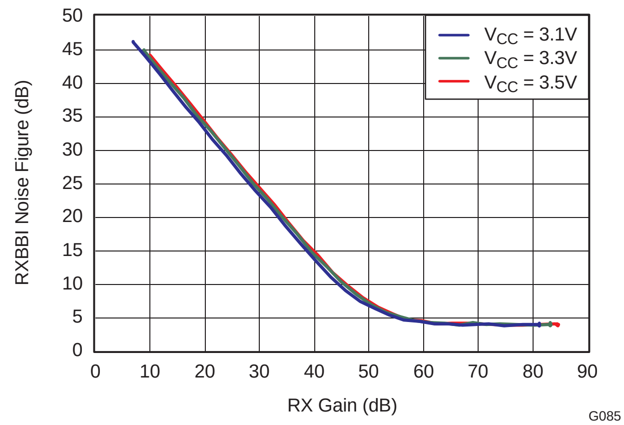


Figure 47.

RECEIVER LOW-PASS FILTER TYPICAL CHARACTERISTICS

(T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

RX LOW-PASS FILTER REJECTION vs FREQUENCY

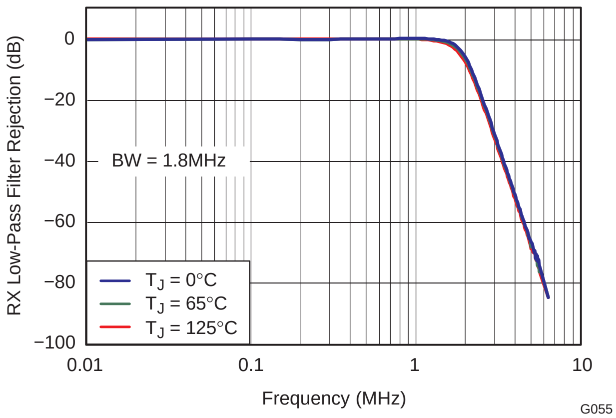


Figure 48.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

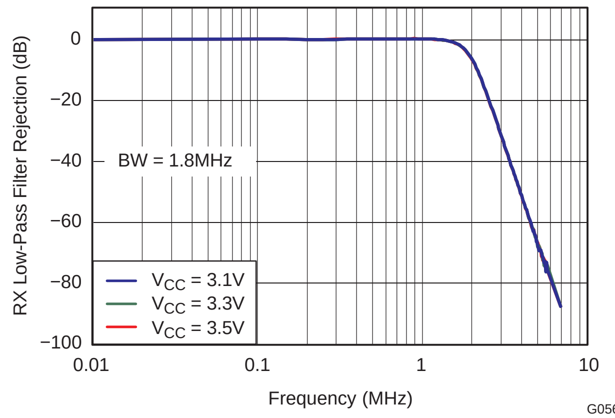


Figure 49.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

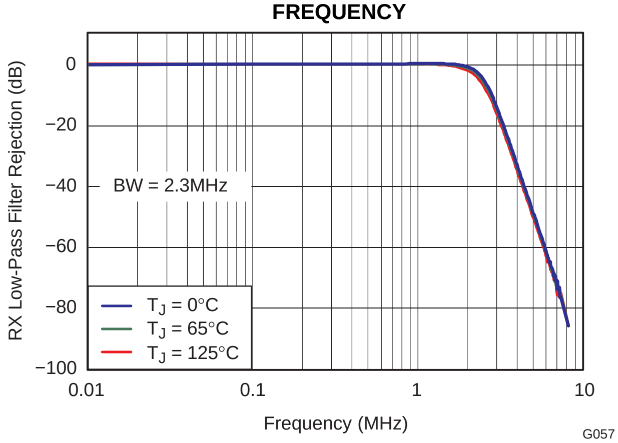


Figure 50.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

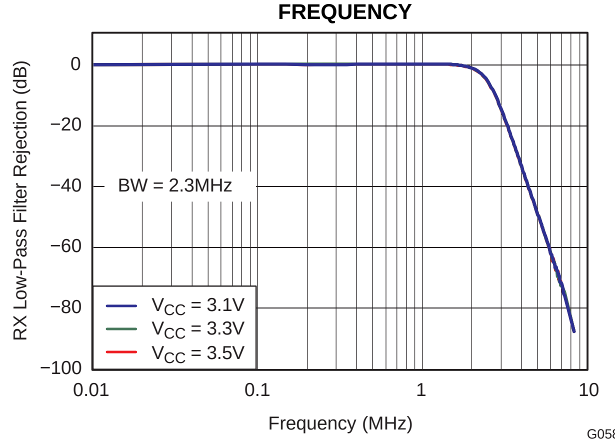


Figure 51.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

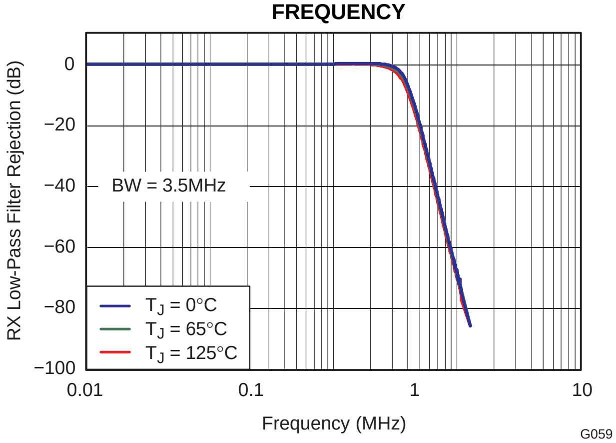


Figure 52.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

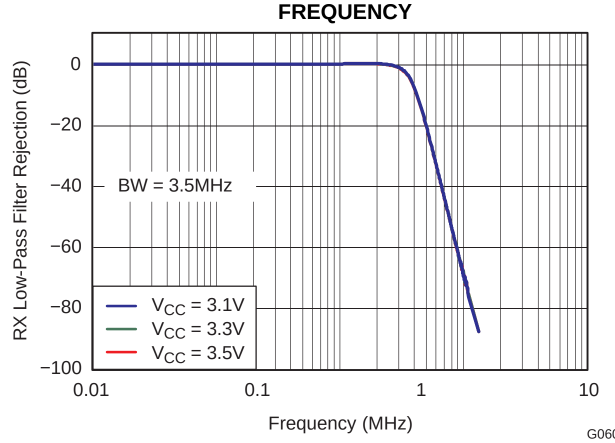


Figure 53.

RECEIVER LOW-PASS FILTER TYPICAL CHARACTERISTICS (continued)

(T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

RX LOW-PASS FILTER REJECTION vs FREQUENCY

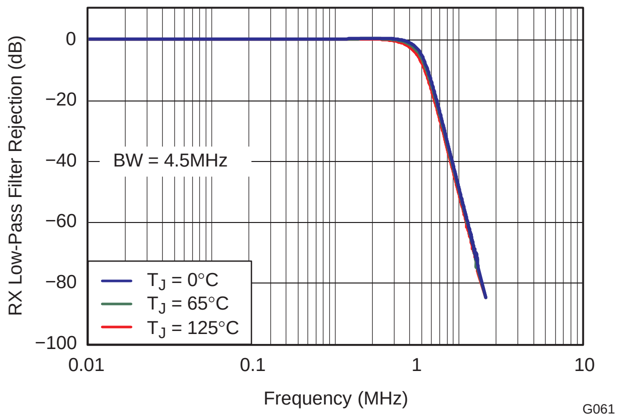


Figure 54.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

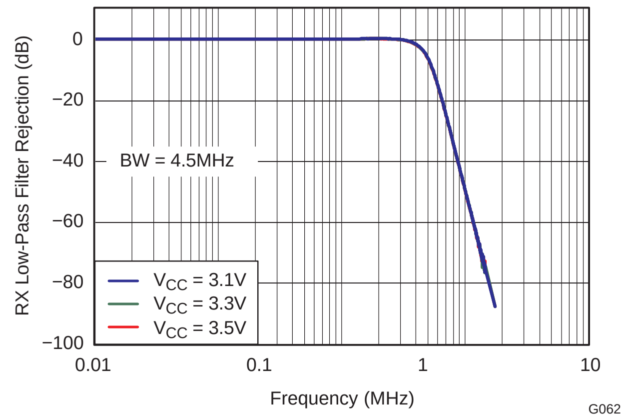


Figure 55.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

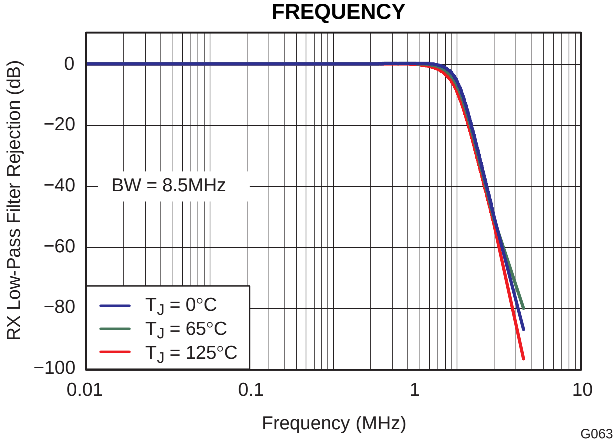


Figure 56.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

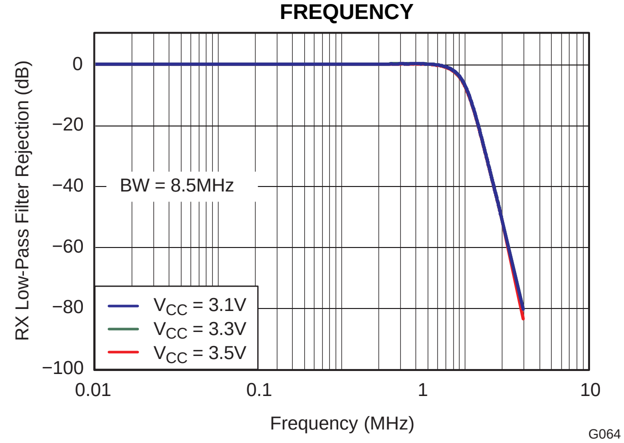


Figure 57.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

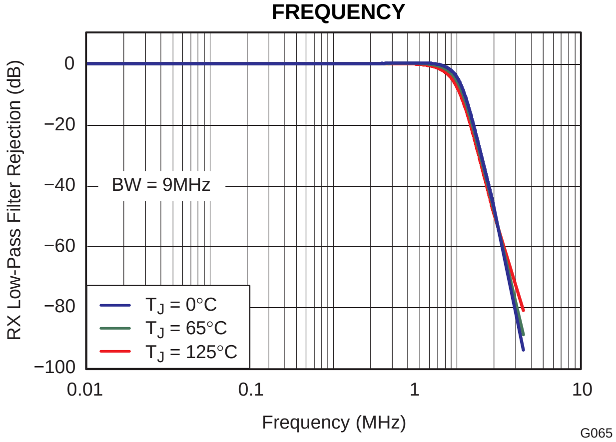


Figure 58.

RX LOW-PASS FILTER REJECTION vs FREQUENCY

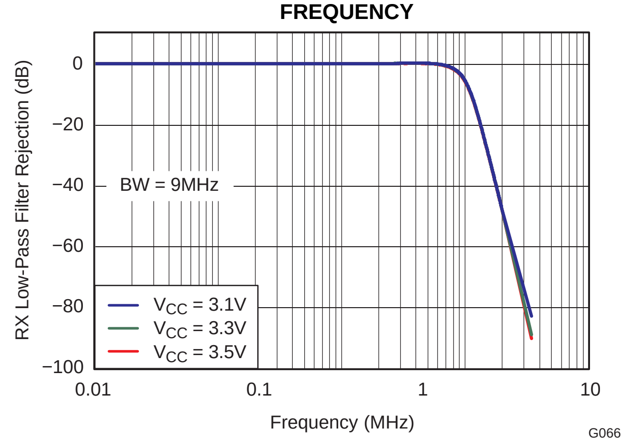


Figure 59.

RECEIVER LOW-PASS FILTER TYPICAL CHARACTERISTICS (continued)

(T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

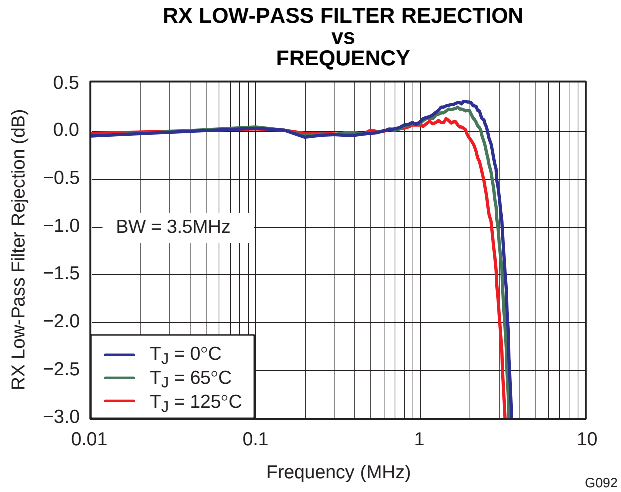


Figure 60.

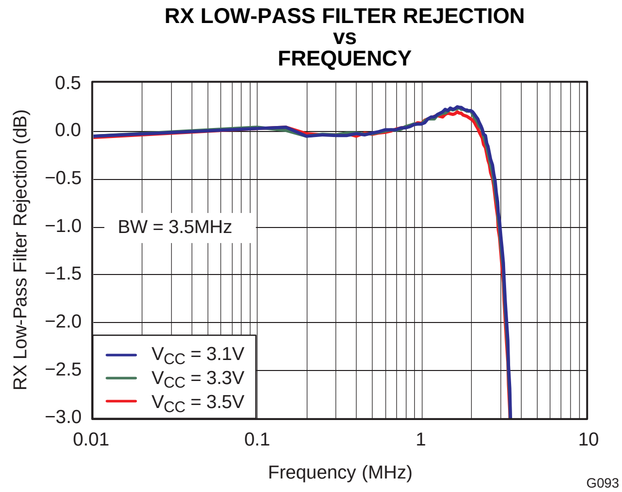


Figure 61.

TRANSMITTER TYPICAL CHARACTERISTICS

Measured after the transformer (0.7-dB insertion loss) and with a TXBBI/TXBBQ input level of –23 dBVrms (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

TX OUTPUT POWER vs TX ATTENUATION SETTING

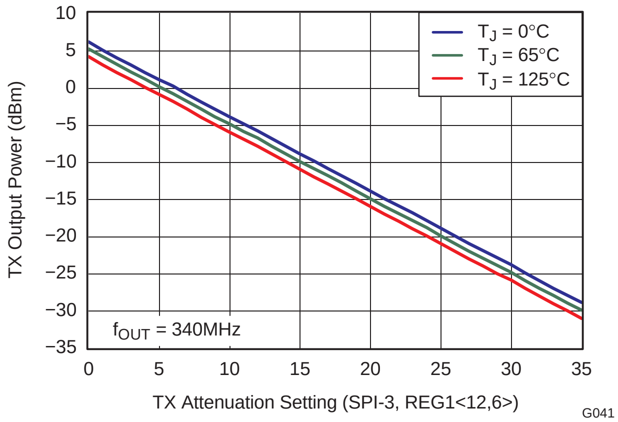


Figure 62.

TX OUTPUT POWER vs TX ATTENUATION SETTING

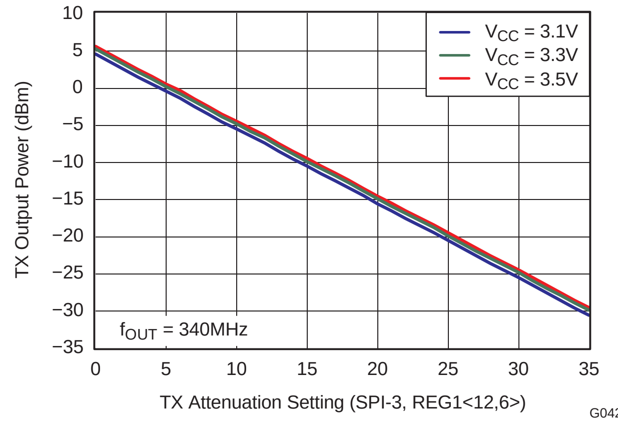


Figure 63.

TX GAIN vs TX ATTENUATION SETTING

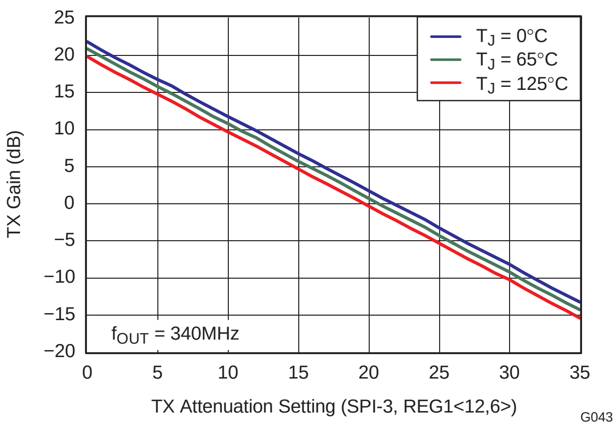


Figure 64.

TX GAIN vs TX ATTENUATION SETTING

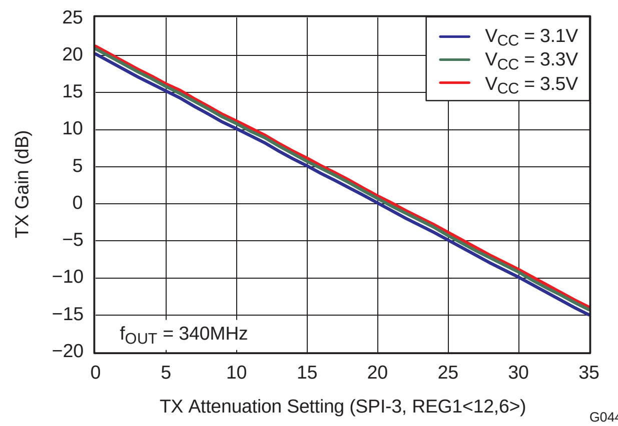


Figure 65.

TX 0.5-dB GAIN STEP vs TX ATTENUATION SETTING

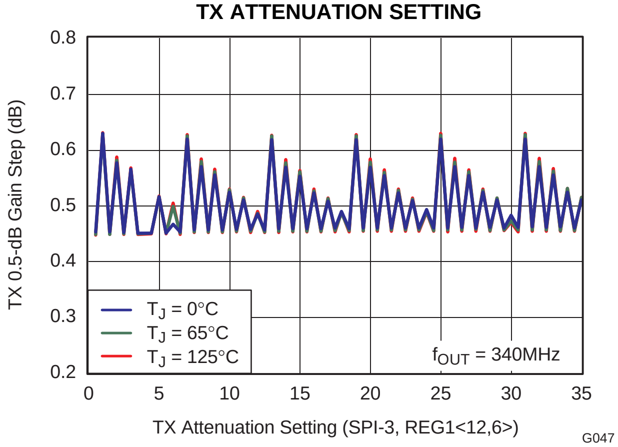


Figure 66.

TX 0.5-dB GAIN STEP vs TX ATTENUATION SETTING

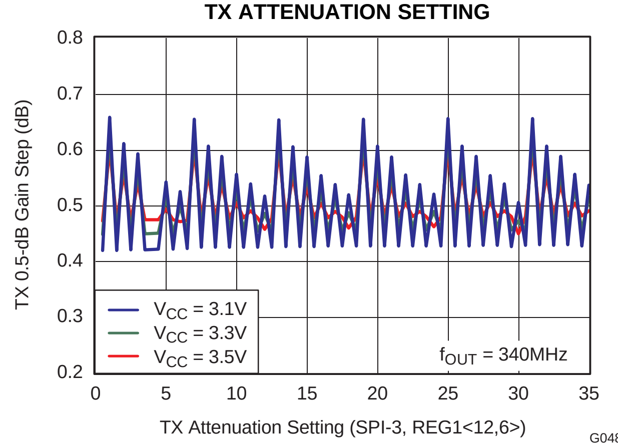


Figure 67.

TRANSMITTER TYPICAL CHARACTERISTICS (continued)

Measured after the transformer (0.7-dB insertion loss) and with a TXBBI/TXBBQ input level of –23 dBVrms (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

TX 1-dB GAIN STEP vs TX ATTENUATION SETTING

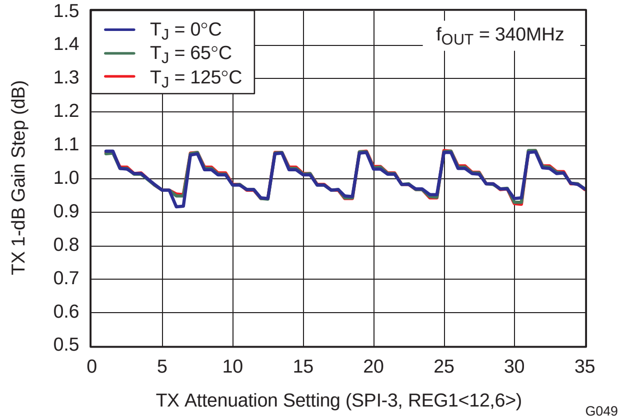


Figure 68.

TX 1-dB GAIN STEP vs TX ATTENUATION SETTING

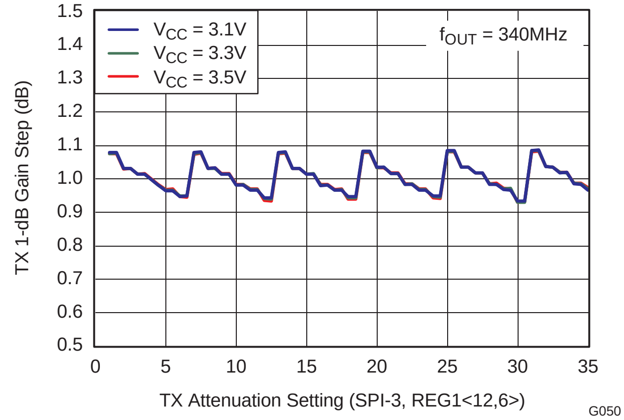


Figure 69.

TX CUMULATIVE GAIN ERROR vs TX ATTENUATION SETTING

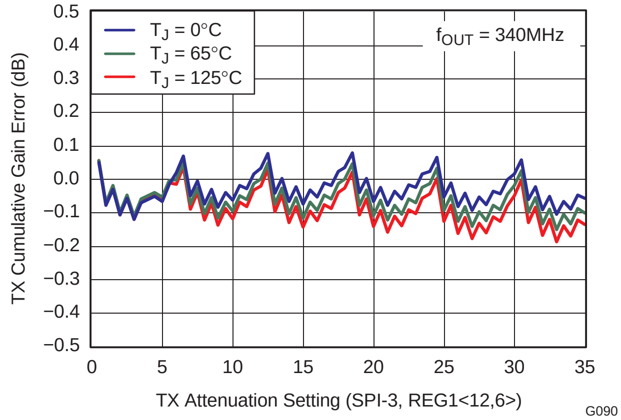


Figure 70.

TX CUMULATIVE GAIN ERROR vs TX ATTENUATION SETTING

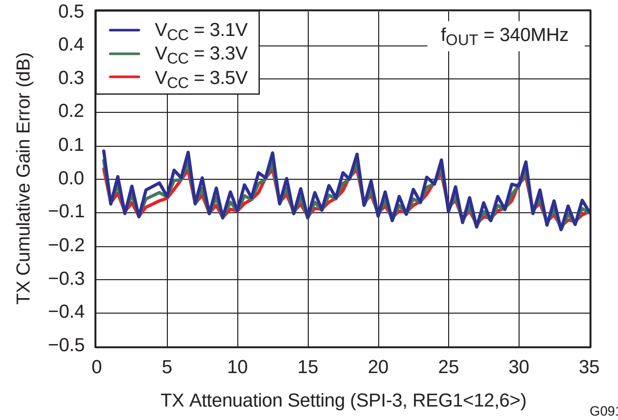


Figure 71.

UNCALIBRATED TX SIDEBAND SUPPRESSION vs TX ATTENUATION SETTING

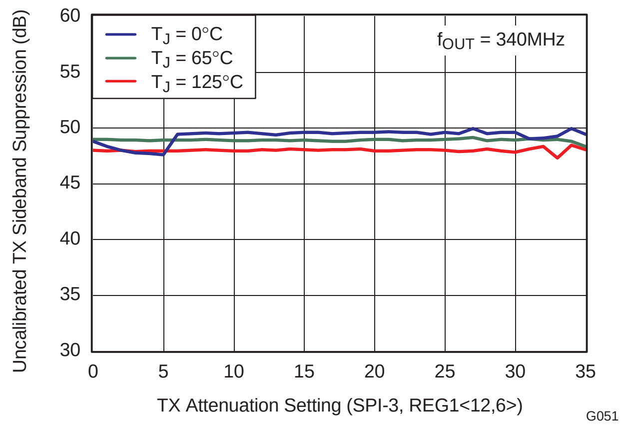


Figure 72.

UNCALIBRATED TX SIDEBAND SUPPRESSION vs TX ATTENUATION SETTING

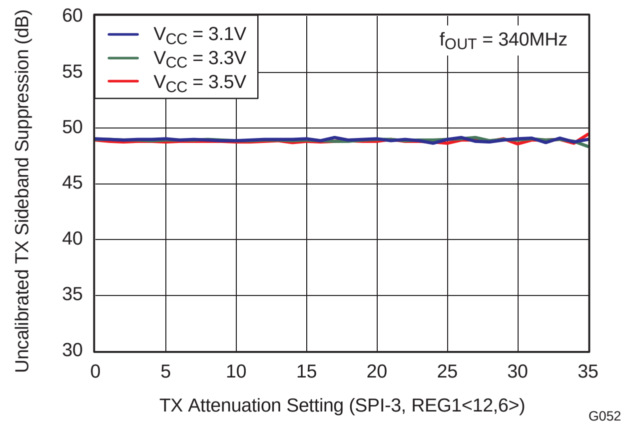


Figure 73.

TRANSMITTER TYPICAL CHARACTERISTICS (continued)

Measured after the transformer (0.7-dB insertion loss) and with a TXBBI/TXBBQ input level of –23 dBVrms (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

TX CARRIER LEAKAGE vs TX ATTENUATION SETTING

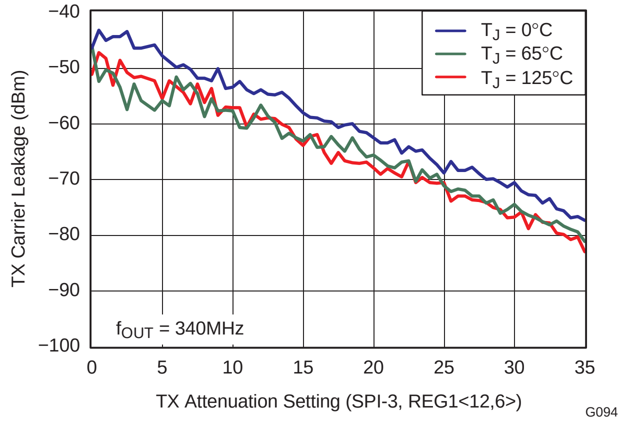


Figure 74.

TX CARRIER LEAKAGE vs TX ATTENUATION SETTING

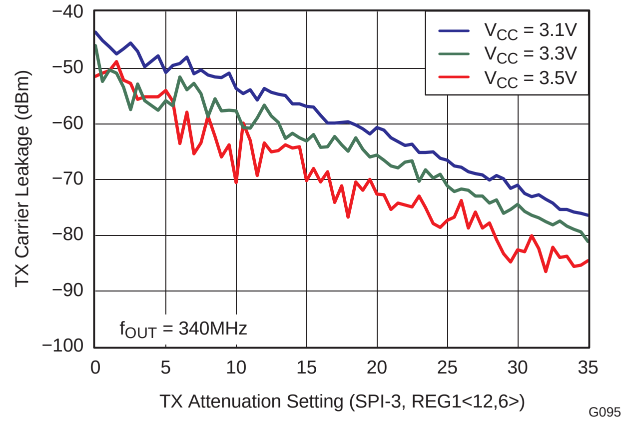


Figure 75.

TX OUTPUT IP3 vs TX ATTENUATION SETTING

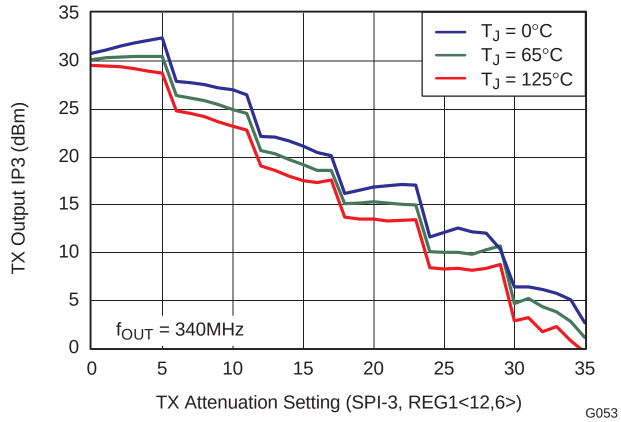


Figure 76.

TX OUTPUT IP3 vs TX ATTENUATION SETTING

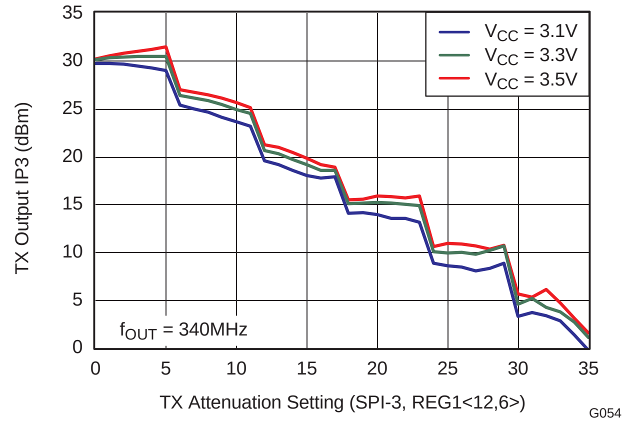


Figure 77.

TX IM3 vs TX ATTENUATION SETTING

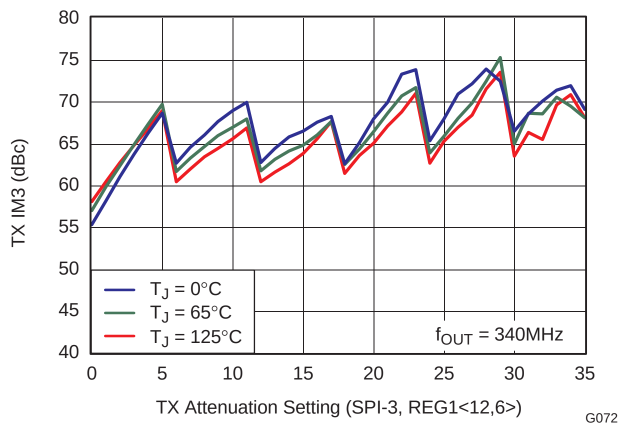


Figure 78.

TX IM3 vs TX ATTENUATION SETTING

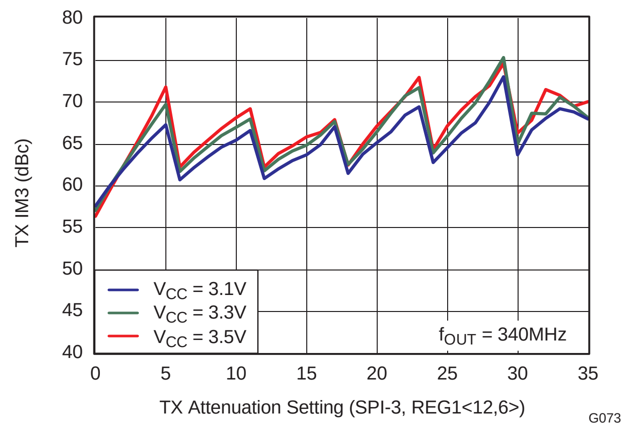


Figure 79.

TRANSMITTER TYPICAL CHARACTERISTICS (continued)

Measured after the transformer (0.7-dB insertion loss) and with a TXBBI/TXBBQ input level of –23 dBVrms (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

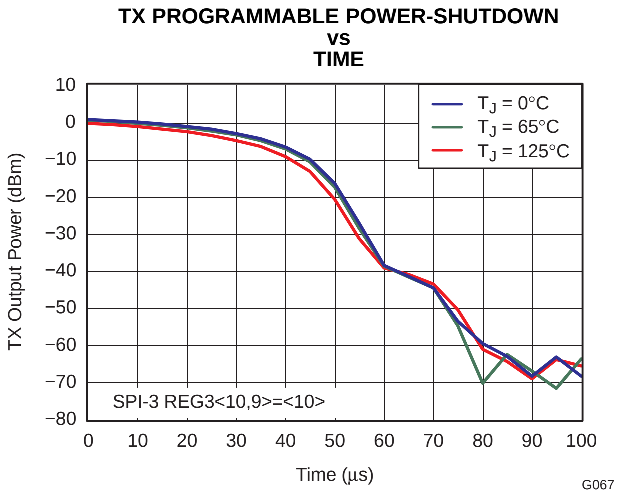


Figure 80.

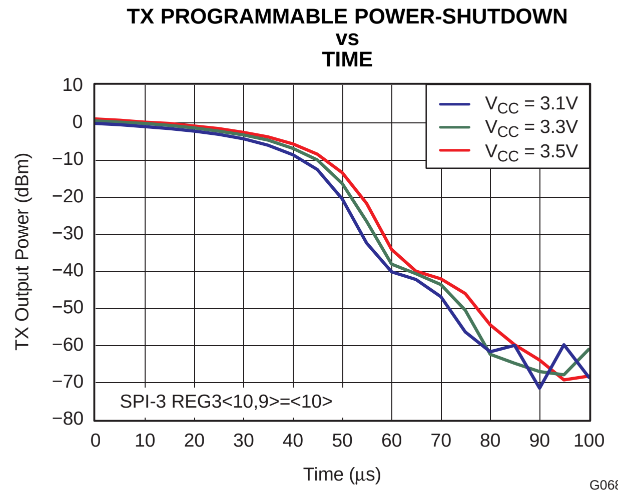


Figure 81.

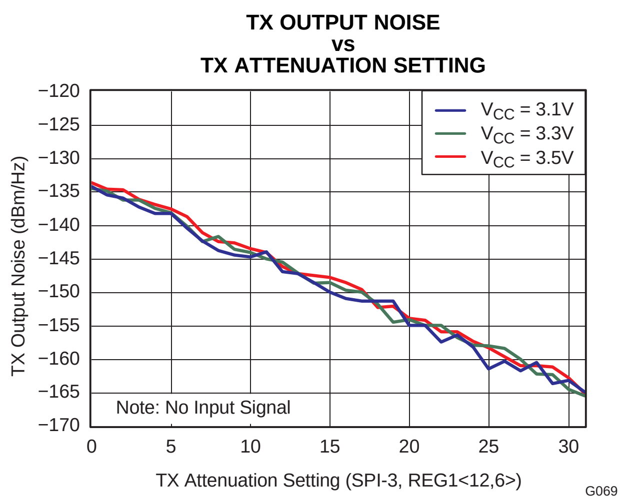


Figure 82.

PLL TYPICAL CHARACTERISTICS

Measured at TXLOTEST pin (6) and RXLOTEST pin (53). Charge-pump current = 1 mA, PFD frequency = 20 MHz, loop filter optimized (see *Application Schematic* section). (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

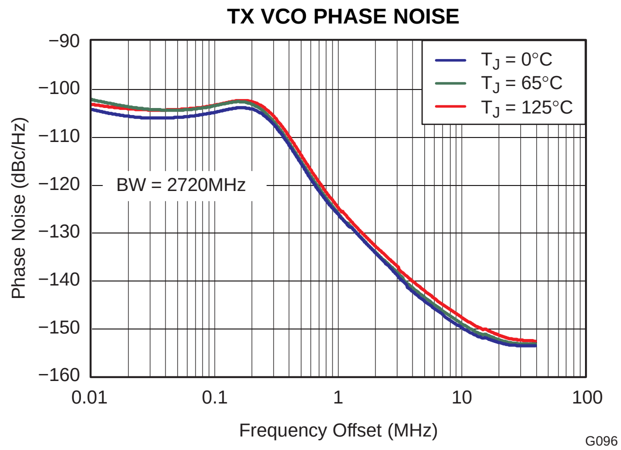


Figure 83.

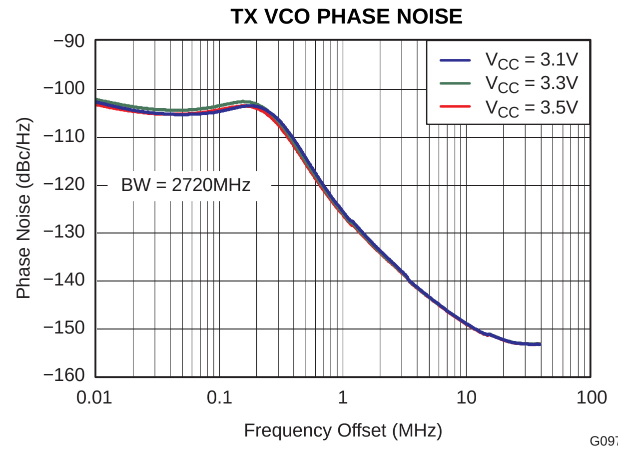


Figure 84.

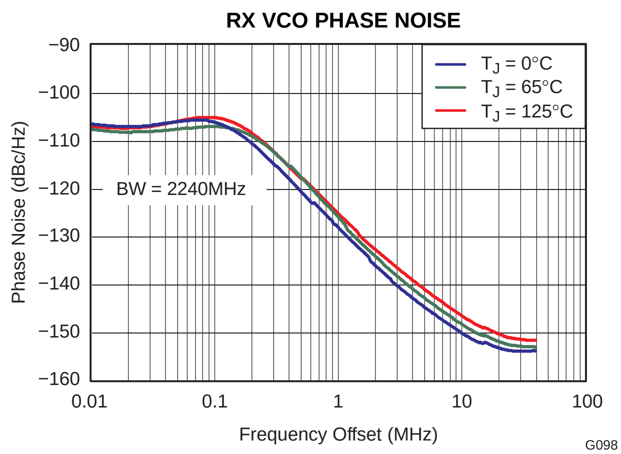


Figure 85.

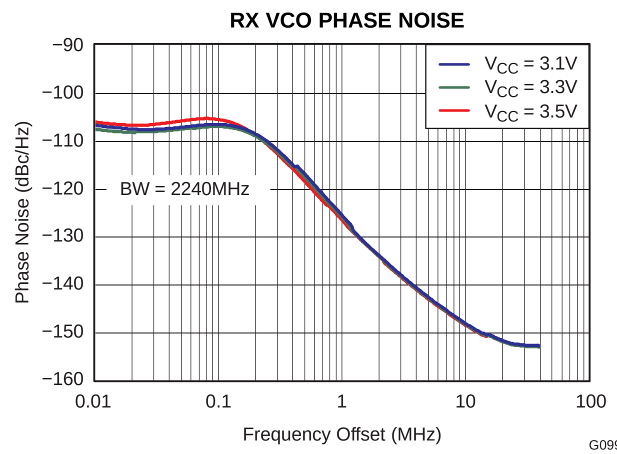


Figure 86.

XPIC RECEIVER TYPICAL CHARACTERISTICS

f_{in}= 140 MHz, XPIC baseband gain setting = 2 (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

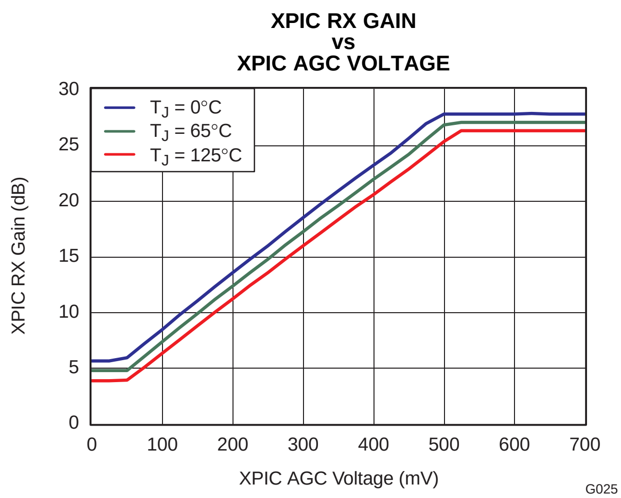


Figure 87.

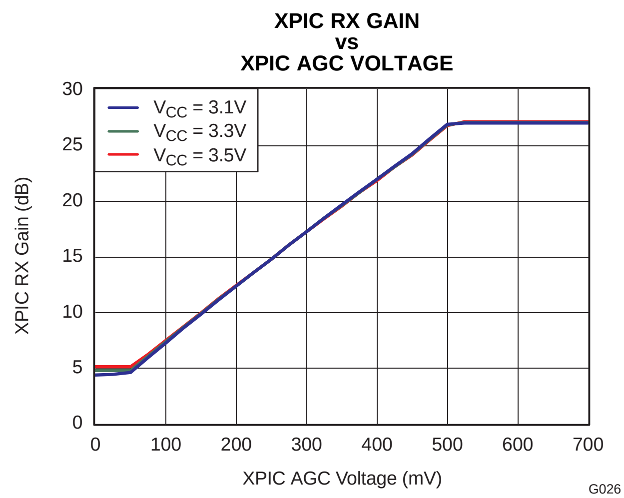


Figure 88.

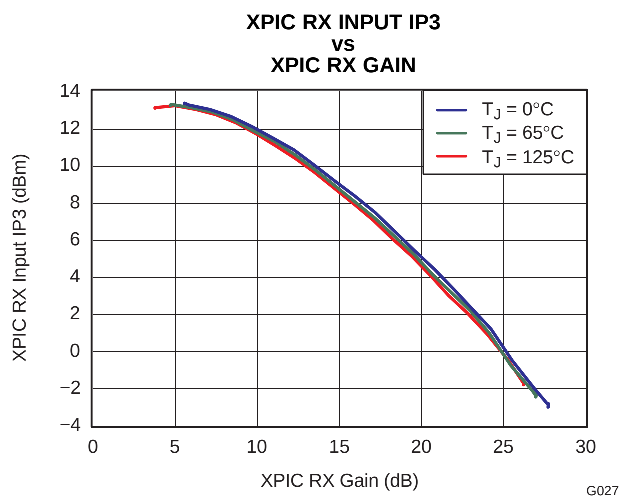


Figure 89.

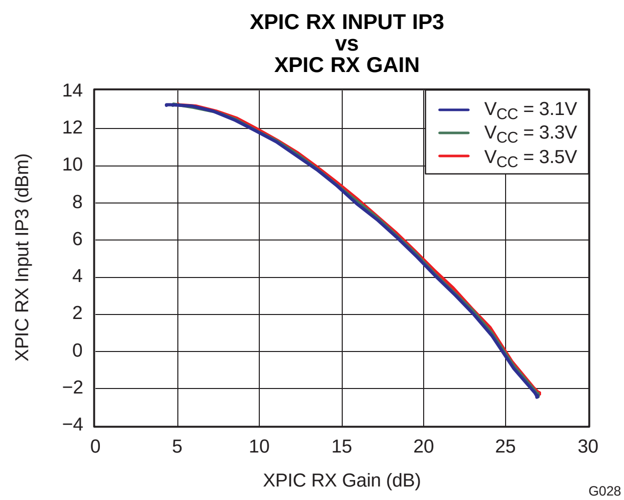


Figure 90.

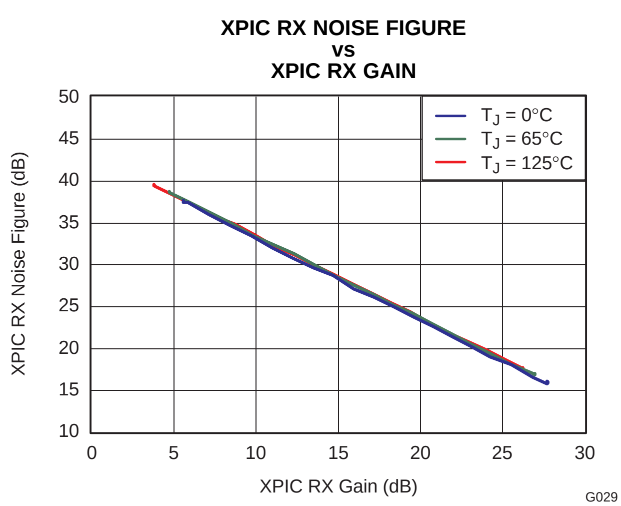


Figure 91.

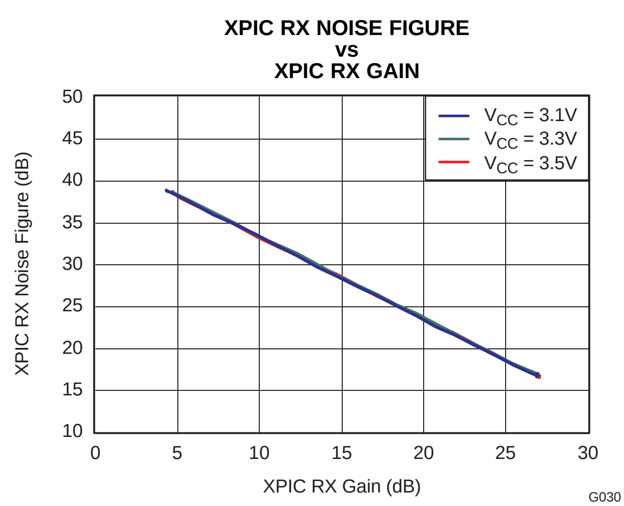


Figure 92.

INSERTION LOSSES TYPICAL CHARACTERISTICS

Measured after transformers (see *Application Schematic* section). (T_J = 65°C, V_{CC} = 3.3 V, unless otherwise noted)

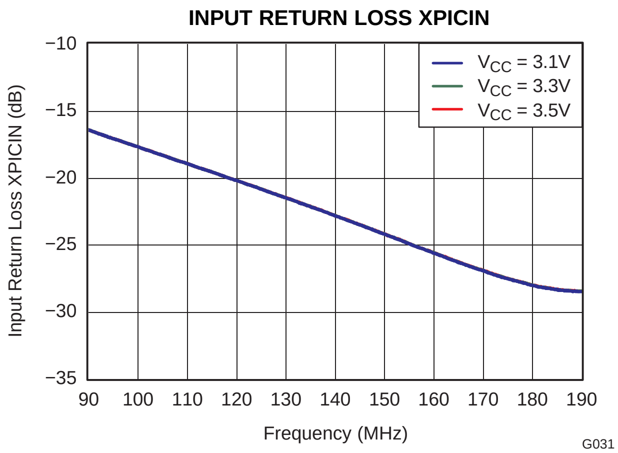


Figure 93.

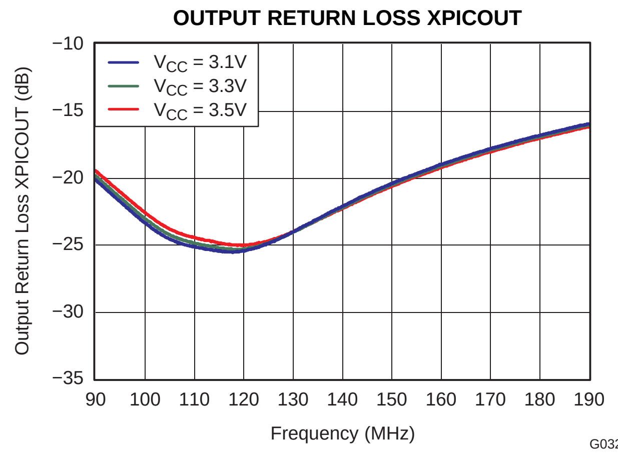


Figure 94.

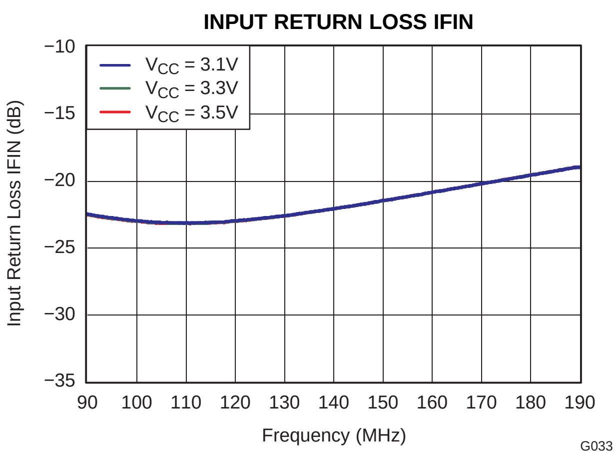


Figure 95.

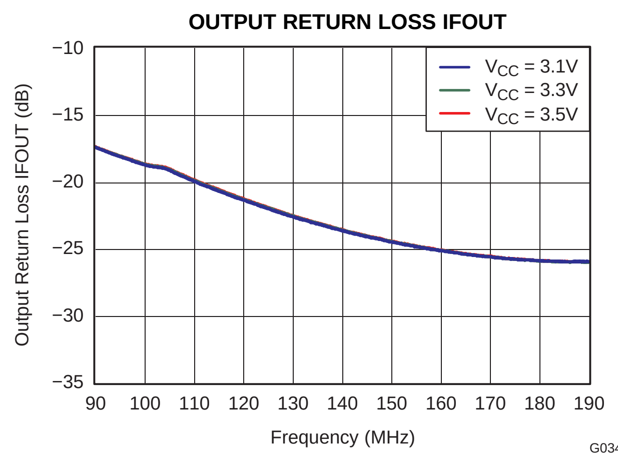


Figure 96.

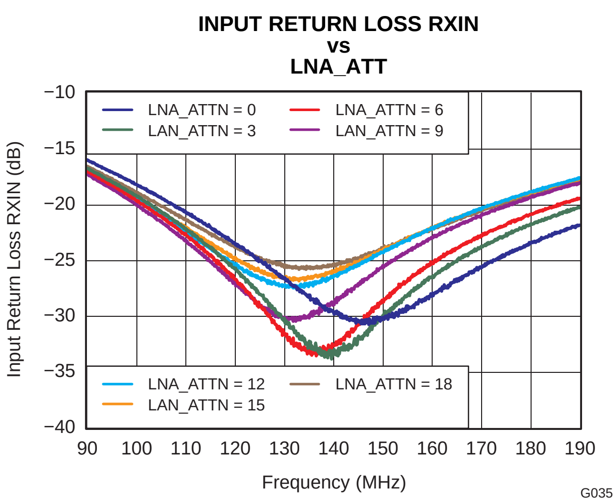


Figure 97.

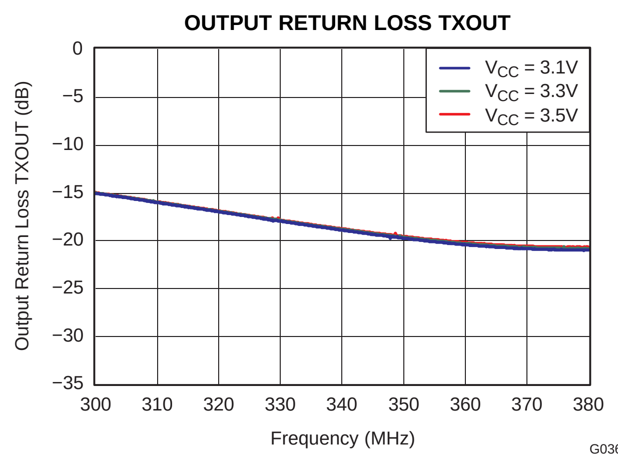


Figure 98.

SPI REGISTERS

The TRF2443 features a three-wire serial programming interface (SPI) that controls an internal 32-bit shift register. There are a total of three signals that must be applied: the clock (CLKSPI), the serial data (DATASPI) and the latch enable (LESPI). The TRF2443 has an additional pin (RDBKSPI) for readback functionality. This pin is a digital pin and can be used to read back values of different internal registers.

The DATA (DB0–DB31) is loaded LSB-first and is read on the rising edge of the CLOCK. The latch enable is asynchronous to the CLOCK, and at its rising edge the data in the shift register is loaded onto the selected internal register. The 5 LSBs of the data field are the address bits to select the available internal registers (see Figure 99).

The SPI can operate reliably at clock speeds up to 20 MHz (clock period <50 ns). In theory, two 32-bit registers could be programmed within 3.3 µs (64 clock cycles at 50 ns per clock cycle plus setup times). However, the user must exercise care when writing consecutive registers to ensure that subsequent register writes do not disrupt a previously requested operation such as a calibration. Calibration times are functions of the external reference frequency used as well as internally programmable clock dividers set by the user. The application section of this data sheet describes how to determine these calibration times. The user should allow for such calibration times when writing registers to the serial interface that contain settings related to the calibration or settings related to the circuits which are being calibrated.

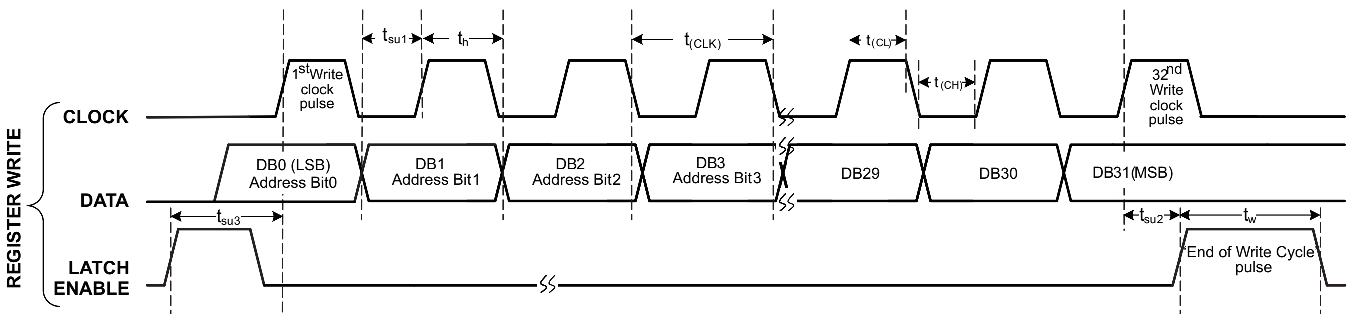


Figure 99. SPI Timing Diagram

Table 1. SPI Timing – Writing Phase

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_h	Hold time, data to clock	20			ns
t_{SU1}	Setup time, data to clock	20			ns
$t_{(CL)}$	Clock low duration	20			ns
$t_{(CH)}$	Clock high duration	20			ns
t_{SU2}	Setup time, clock to enable	20			ns
t_W	Enable Time	50			ns
$t_{(CLK)}$	Clock period	50			ns
t_{SU3}	Setup time, latch to data	70			ns

TRF2443 Addressing Scheme

The TRF2443 has a separate set of register banks for the EEPROM (SPI-0), TX PLL (SPI-1), RX PLL (SPI-2), and TX/RX functionality (SPI-3). Each of the register banks has unique address bits to identify it, and within each register bank there are several registers which require an additional 3 bits of addressing.

Each register is 32 bits long; the bits can be described by B<31,0>. The 5 LSBs of each register, (B<4,0>), are the address bits, with B<4,3> corresponding to the address of the register bank and B<2,0> corresponding to the address of the individual register within each bank (see Table 2).

Table 2. SPI Register Bank Addresses

REGISTER BANK	ADDRESS	NUMBER OF REGISTERS
EEPROM	00	3
TX PLL	01	6
RX PLL	10	6
TX/RX	11	8

Table 3. SPI Register Addresses

		NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Address bits	B0	ADDR <0>	X	X	**Register address: B<2,0>**
	B1	ADDR <1>	X	X	**For PLLs (SPI-1 and SPI-2):**
	B2	ADDR <2>	X	X	Reg 0(000), Reg 1(001), Reg 2 (010), Reg 3 (011), Reg 4 (100), Reg 5 (101)
					For TX_RX (SPI-3): Reg 0 (000), Reg 1(001), Reg 2 (010), Reg 3 (011), Reg 4 (100), Reg 5 (101), Reg 6(110), Reg 7(111) (***Note:*** *In TX_RX (SPI-3), Reg 0 has special functionality as described in the TX and RX SPI Registers section.*)
	B3	ADDR <3>	X	X	Register bank: B<4,3>
	B4	ADDR <4>	X	X	TX PLL (01); RX PLL (10); TX_RX (11)
Data field	B5	Data bit (LSB)	X	X	
	B6	Data bit	X	X	
	B7	Data bit	X	X	
	B8	Data bit	X	X	
	B9	Data bit	X	X	
	B10	Data bit	X	X	
	B11	Data bit	X	X	
	B12	Data bit	X	X	
	B13	Data bit	X	X	
	B14	Data bit	X	X	
	B15	Data bit	X	X	
	B16	Data bit	X	X	
	B17	Data bit	X	X	
	B19	Data bit	X	X	
	B20	Data bit	X	X	
	B21	Data bit	X	X	
	B22	Data bit	X	X	
	B23	Data bit	X	X	
	B24	Data bit	X	X	
	B25	Data bit	X	X	
	B26	Data bit	X	X	
	B27	Data bit	X	X	
	B28	Data bit	X	X	
	B29	Data bit	X	X	
	B30	Data bit	X	X	
	B31	Data bit (MSB)	X	X	

TX Synthesizer SPI registers

SPI1 Register 1

Register address			SPI address		TX reference divider										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

TX reference divider			REF INV	VCO NEG	TX charge-pump current					TX CP DOUBLE	RSV	RSB	CP OFF	CP UP	CP DN
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 1	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	1	1	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	0	0	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	0	0	
Bit5	TXRDIV_0	0	App. specific	14-bit reference divider value (minimum value Rmin = 1; maximum value Rmax = 16,383)
Bit6	TXRDIV_1	0	App. specific	
Bit7	TXRDIV_2	0	App. specific	
Bit8	TXRDIV_3	0	App. specific	
Bit9	TXRDIV_4	0	App. specific	
Bit10	TXRDIV_5	0	App. specific	
Bit11	TXRDIV_6	0	App. specific	
Bit12	TXRDIV_7	0	App. specific	
Bit13	TXRDIV_8	0	App. specific	
Bit14	TXRDIV_9	0	App. specific	
Bit15	TXRDIV_10	0	App. specific	
Bit16	TXRDIV_11	0	App. specific	
Bit17	TXRDIV_12	0	App. specific	
Bit18	TXRDIV_13	0	App. specific	
Bit19	TXREF_INV	0	0	Invert reference-clock polarity; 1 = use falling edge
Bit20	TXNEG_VCO	1	1	VCO polarity control; 1 = negative slope (negative K_v)
Bit21	TXICP_0	0	0	Program charge-pump dc current, I_{CP}, from 0.5 mA (1 1111) to 2 mA (0 0000); default value 1 mA (0 1010)
Bit22	TXICP_1	1	1	
Bit23	TXICP_2	0	0	
Bit24	TXICP_3	1	1	
Bit25	TXICP_4	0	0	
Bit26	TXICPDOUBLE	0	0	1 = set I_{CP} to double the current
Bit27	RSV	0	0	Reserved
Bit28	RSV	0	0	Reserved
Bit29	TXCP_OVERRIDE	0	0	1 = disable charge pump
Bit30	TXCP_UP	0	0	1 = enable the charge-pump source current in disable mode
Bit31	TXCP_DN	0	0	1 = enable the charge-pump sink current in disable mode

SPI1 Register 2

Register address			SPI address		TX N-divider value										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
TX N-divider value					RSV					DIV 8–16	CAL clock divider			CAL SEL	EN CAL
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 2	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	0	0	Register address bits
Bit1	ADDR_1	1	1	
Bit2	ADDR_2	0	0	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	0	0	
Bit5	TX_NINT_0	0	App. specific	TX PLL N-divider division setting Power-On value = 68 (<0000 0000 0100 0100) → f_{VCO} = 2720 MHz (with f_{PFD} = 20 MHz) f_{out} = 340 MHz (minimum value N_{min} = 56; maximum value N_{max} = 65,535)
Bit6	TX_NINT_1	0	App. specific	
Bit7	TX_NINT_2	1	App. specific	
Bit8	TX_NINT_3	0	App. specific	
Bit9	TX_NINT_4	0	App. specific	
Bit10	TX_NINT_5	0	App. specific	
Bit11	TX_NINT_6	1	App. specific	
Bit12	TX_NINT_7	0	App. specific	
Bit13	TX_NINT_8	0	App. specific	
Bit14	TX_NINT_9	0	App. specific	
Bit15	TX_NINT_10	0	App. specific	
Bit16	TX_NINT_11	0	App. specific	
Bit17	TX_NINT_12	0	App. specific	
Bit18	TX_NINT_13	0	App. specific	
Bit19	TX_NINT_14	0	App. specific	
Bit20	TX_NINT_15	0	App. specific	
Bit21	RSV	0	0	Reserved
Bit22	RSV	0	0	Reserved
Bit23	RSV	0	0	Reserved
Bit24	RSV	0	0	Reserved
Bit25	RSV	1	1	Reserved
Bit26	TXDIV_SEL	1	1	TX VCO divider selection (1 = divide by 8; 0 = divide by 16)
Bit27	TXCAL_CLK_0	1	1	Set the clock speed used in the TX VCO frequency autocalibration. The clock is derived from the reference clock through a frequency divider.
Bit28	TXCAL_CLK_1	0	0	
Bit29	TXCAL_CLK_2	1	1	
Bit30	TXCAL_SEL	0	1	Select the TX VCO frequency calibration mode (1 = autocalibration; 0 = manual)
Bit31	EN_TXCAL	0	1	Enable TX VCO frequency autocalibration (1 → start)

TXCAL_CLK<2,0>: Set the frequency divider value used to derive the TX VCO calibration clock from the reference clock (See Table 4)

Table 4. TX VCO Calibration Clock Divider vs TXCAL_CLK<2,0>

TXCAL_CLK	FREQUENCY DIVIDER
000	1
001	8
010	16
011	128
100	256
101	1024
110	2048
111	16,684

SPI1 Register 4

Register address			SPI address		RSV	RSV	RSV	RSV	RSV	RSV	Power down TX PLL blocks				RSV
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

RSV	Power down TX PLL blocks						RSV	RSV	RSV	TXVCO trim					
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 4	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	0	0	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	1	1	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	0	0	
Bit5	RSV	0	0	Reserved
Bit6	RSV	0	0	Reserved
Bit7	RSV	0	0	Reserved
Bit8	RSV	0	0	Reserved
Bit9	RSV	1	1	Reserved
Bit10	RSV	1	1	Reserved
Bit11	PWD_TXCP	0	0	When 1, TX charge pump is off
Bit12	PWD_TXVCO	0	0	When 1, TX VCO is off
Bit13	PWD_TXBUF1	0	0	Power down VCO buffer 1 (1 = off)
Bit14	PWD_TXBUF2	0	0	Power down VCO buffer 2 (1 = off)
Bit15	RSV	1	1	Reserved
Bit16	PWD_TX_TESTBUF	0	1	Power down TXVCO output buffer, pin TXLOTEST (1 = off)
Bit17	PWD_TXDIV2	0	0	Power down VCO divider (1 = off)
Bit18	PWD_TXPRESC	0	0	Power down prescaler buffer (1 = off)
Bit19	PWD_TXRESYNC	0	0	Power down re-synch D flip-flop (1 = off)
Bit20	PWD_TXPLL	0	0	Power down whole TX PLL (1 = off)
Bit21	PWD_TXDIV	0	0	Power down LO divider (1 = off)
Bit22	PWD_TXDET	0	0	Power down VCO detector (1 = off; used for VCO calibration)
Bit23	RSV	0	0	Reserved
Bit24	RSV	0	0	Reserved
Bit25	RSV	0	0	Reserved

REGISTER 4	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit26	TXVCO_TRIM_0	0	0	VCO coarse-frequency tuning control (manual mode)
Bit27	TXVCO_TRIM_1	0	0	
Bit28	TXVCO_TRIM_2	0	0	
Bit29	TXVCO_TRIM_3	0	0	
Bit30	TXVCO_TRIM_4	0	0	
Bit31	TXVCO_TRIM_5	0	0	

SPI1 Register 5

Register address			SPI address		TXPLL bias			RSV	RSV	TXVCO bias				BUF1 bias	
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

BUF2 bias		OUTBUF bias		PRESC bias		BIAS SEL	VCO CAL REF			RSV	RSV	RSV	RSV	RSV	RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 5	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	1	1	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	1	1	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	0	0	
Bit5	TXPLL_BIAS_0	0	0	TX PLL reference-current control bits. Adjust reference current from 40 μA to 60 μA. Suggested value is 52 μA (100).
Bit6	TXPLL_BIAS_1	0	0	
Bit7	TXPLL_BIAS_2	1	1	
Bit8	RSV	0	0	Reserved
Bit9	RSV	0	0	Reserved
Bit10	TXVCO_BIAS_0	0	0	TX VCO bias control bits. VCO current can be changed from 10 mA (0000) to 25 mA (1111), 1-mA step. Suggested value is 18 mA (1000).
Bit11	TXVCO_BIAS_1	0	0	
Bit12	TXVCO_BIAS_2	0	0	
Bit13	TXVCO_BIAS_3	1	1	
Bit14	TXBUF1_BIAS_0	0	0	It sets the PLL buffer-1 bias from 0.8 mA (00) to 2 mA (11), 0.4-mA step. Suggested value is 1.6 mA (10).
Bit15	TXBUF1_BIAS_1	1	1	
Bit16	TXBUF2_BIAS_0	0	0	It sets the PLL buffer-2 bias from 0.8 mA (00) to 2 mA (11), 0.4-mA step. Suggested value is 1.6 mA (10).
Bit17	TXBUF2_BIAS_1	1	1	
Bit18	TXBUFOUT_BIAS_0	0	0	TXPLL output-buffer reference bias current. 200 μA (00) to 500 μA (11). Suggested value is 400 μA (10).
Bit19	TXBUFOUT_BIAS_1	1	1	
Bit20	TXPRES_BIAS_0	1	0	TXPLL prescaler reference bias current. 200 μA (00) to 500 μA (11). Suggested value is 400 μA (10).
Bit21	TXPRES_BIAS_1	1	1	
Bit22	TXVCO_CAL_IB	0	1	Select bias current type for VCO calibration circuitry 1 = PTAT; 0 = constant over temperature
Bit23	TXVCO_CAL_REF_0	0	1	TX VCO calibration reference-voltage trimming.
Bit24	TXVCO_CAL_REF_1	0	1	000 → 1.175 V
Bit25	TXVCO_CAL_REF_2	0	0	111 → 2.05 V. Suggested value is 1.55 V (011).
Bit26	RSV	0	0	Reserved
Bit27	RSV	0	0	Reserved
Bit28	RSV	0	0	Reserved
Bit29	RSV	0	0	Reserved
Bit30	RSV	0	0	Reserved
Bit31	RSV	0	0	Reserved

RX Synthesizer SPI registers

SPI2 Register 1

Register address			SPI address		RX reference divider										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

—			REF INV	VCO NEG	RX charge-pump current					RX CP DOUBLE	RSV	RSV	CP OFF	CP UP	CP DN
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 1	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	1	1	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	0	0	
Bit3	ADDR_3	0	0	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	RXRDIV_0	0	App. specific	14-bit reference-divider value (minimum value R_{min} = 1; maximum value R_{max} = 16,383)
Bit6	RXRDIV_1	0	App. specific	
Bit7	RXRDIV_2	0	App. specific	
Bit8	RXRDIV_3	0	App. specific	
Bit9	RXRDIV_4	0	App. specific	
Bit10	RXRDIV_5	0	App. specific	
Bit11	RXRDIV_6	0	App. specific	
Bit12	RXRDIV_7	0	App. specific	
Bit13	RXRDIV_8	0	App. specific	
Bit14	RXRDIV_9	0	App. specific	
Bit15	RXRDIV_10	0	App. specific	
Bit16	RXRDIV_11	0	App. specific	
Bit17	RXRDIV_12	0	App. specific	
Bit18	RXRDIV_13	0	App. specific	
Bit19	RXREF_INV	0	0	Invert reference-clock polarity; 1 = use falling edge
Bit20	RXNEG_VCO	1	1	VCO polarity control; 1 = negative slope (negative K_v)
Bit21	RXICP_0	0	0	Program charge-pump dc current, I_{CP} from 0.5 mA (1 1111) to 2 mA (0 0000); default value 1 mA (0 1010)
Bit22	RXICP_1	1	1	
Bit23	RXICP_2	0	0	
Bit24	RXICP_3	1	1	
Bit25	RXICP_4	0	0	
Bit26	RXICPDOUBLE	0	0	1 = set I_{CP} to double the current
Bit27	RSV	0	0	Reserved
Bit28	RSV	0	0	Reserved
Bit29	RXCP_OVERRIDE	0	0	1 = disable charge pump
Bit30	RXCP_UP	0	0	1 = enable the charge-pump source current in disable mode
Bit31	RXCP_DN	0	0	1 = enable the charge-pump sink current in disable mode

SPI2 REGISTER 2

Register address			SPI address		RX N-divider value										
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

RX N-divider value					RSV					DIV 8–16	CAL clock divider			CAL SEL	EN CAL
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 2	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	0	0	Register address bits
Bit1	ADDR_1	1	1	
Bit2	ADDR_2	0	0	
Bit3	ADDR_3	0	0	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	RX_NINT_0	0	App. specific	RX PLL N-divider division setting Power-On value = 112 (<00 000 000 0111 0000>) → f_{VCO} = 2240 MHz (with f_{PFD} = 20 MHz) f_{out} = 140 MHz (minimum value N_{min} = 56; maximum value N_{max} = 65,535)
Bit6	RX_NINT_1	0	App. specific	
Bit7	RX_NINT_2	0	App. specific	
Bit8	RX_NINT_3	0	App. specific	
Bit9	RX_NINT_4	1	App. specific	
Bit10	RX_NINT_5	1	App. specific	
Bit11	RX_NINT_6	1	App. specific	
Bit12	RX_NINT_7	0	App. specific	
Bit13	RX_NINT_8	0	App. specific	
Bit14	RX_NINT_9	0	App. specific	
Bit15	RX_NINT_10	0	App. specific	
Bit16	RX_NINT_11	0	App. specific	
Bit17	RX_NINT_12	0	App. specific	
Bit18	RX_NINT_13	0	App. specific	
Bit19	RX_NINT_14	0	App. specific	
Bit20	RX_NINT_15	0	App. specific	
Bit21	RSV	0	0	Reserved
Bit22	RSV	0	0	Reserved
Bit23	RSV	0	0	Reserved
Bit24	RSV	0	0	Reserved
Bit25	RSV	1	1	Reserved
Bit26	RXDIV_SEL	0	0	RX VCO divider selection (1 = divide by 8; 0 = divide by 16)
Bit27	RXCAL_CLK_0	1	1	Set the clock speed used in the RX VCO frequency autocalibration. The clock is derived from the reference clock through a frequency divider.
Bit28	RXCAL_CLK_1	0	0	
Bit29	RXCAL_CLK_2	1	1	
Bit30	RXCAL_SEL	0	1	Select the RX VCO frequency calibration mode (1 = autocalibration; 0 = manual)
Bit31	EN_RXCAL	0	1	Enable RX VCO frequency autocalibration (1 → start)

RXCAL_CLK<2,0>: Set the frequency divider value used to derive the TX VCO calibration clock from the reference clock (See Table 5).

Table 5. RX VCO Calibration Clock Divider vs. RXCAL_CLK<2,0>

RXCAL_CLK	FREQUENCY DIVIDER
000	1
001	8
010	16
011	128
100	256
101	1024
110	2048
111	16,684

SPI2 Register 4

Register address			SPI address		RSV	RSV	RSV	RSV	RSV	RSV	Power down RX PLL blocks				RSV
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

RSV	Power down RX PLL blocks						RSV	RSV	RXVCO trim						
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 4	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	0	0	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	1	1	
Bit3	ADDR_3	0	0	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	RSV	0	0	Reserved
Bit6	RSV	0	0	Reserved
Bit7	RSV	0	0	Reserved
Bit8	RSV	0	0	Reserved
Bit9	RSV	1	1	Reserved
Bit10	RSV	1	1	Reserved
Bit11	PWD_RXCP	0	0	When 1, RX charge pump is off
Bit12	PWD_RXVCO	0	0	When 1, RX VCO is off
Bit13	PWD_RXBUF1	0	0	Power down VCO buffer 1 (1 = off)
Bit14	PWD_RXBUF2	0	0	Power down VCO buffer 2 (1 = off)
Bit15	RSV	1	1	Reserved
Bit16	PWD_RX_TESTBUF	0	1	Power down RXVCO output buffer, pin RXLOTEST (1 = off)
Bit17	PWD_RXDIV2	0	0	Power down VCO divider (1 = off)
Bit18	PWD_RXPRESC	0	0	Power down prescaler buffer (1 = off)
Bit19	PWD_RXRESYNC	0	0	Power down re-synch D flip-flop (1 = off)
Bit20	PWD_RXPLL	0	0	Power down whole RX PLL (1 = off)
Bit21	PWD_RXDIV	0	0	Power down LO divider (1 = off)
Bit22	PWD_RXDET	0	0	Power down VCO detector (1 = off; used for VCO calibration)
Bit23	RSV	0	0	Reserved
Bit24	RSV	0	0	Reserved
Bit25	RXVCO_TRIM_0	0	0	VCO coarse frequency tuning control (manual mode)
Bit26	RXVCO_TRIM_1	0	0	
Bit27	RXVCO_TRIM_2	0	0	
Bit28	RXVCO_TRIM_3	0	0	
Bit29	RXVCO_TRIM_4	0	0	
Bit30	RXVCO_TRIM_5	0	0	
Bit31	RXVCO_TRIM_6	0	0	

SPI2 Register 5

Register address			SPI address		RXPLL BIAS			RSV	RSV	RXVCO BIAS				BUF1 BIAS	
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

BUF2 BIAS		OUTBUF BIAS		PRESC BIAS		BIAS SEL	VCO CAL REF			RSV	RSV	RSV	RSV	RSV	RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 5	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	1	1	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	1	1	
Bit3	ADDR_3	0	0	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	RXPLL_BIAS_0	0	0	RX PLL reference-current control bits. Adjust reference current from 40 μA to 60 μA.
Bit6	RXPLL_BIAS_1	0	0	
Bit7	RXPLL_BIAS_2	1	1	
Bit8	RSV	0	0	Reserved
Bit9	RSV	0	0	Reserved
Bit10	RXVCO_BIAS_0	0	1	RX VCO bias-control bits. VCO current can be changed from 10 mA (0000) to 25 mA (1111), 1-mA steps.
Bit11	RXVCO_BIAS_1	0	1	
Bit12	RXVCO_BIAS_2	0	1	
Bit13	RXVCO_BIAS_3	1	1	
Bit14	RXBUF1_BIAS_0	0	0	It sets the PLL buffer 1 bias from 0.8 mA (00) to 2 mA (11), 0.4-mA steps.
Bit15	RXBUF1_BIAS_1	1	1	
Bit16	RXBUF2_BIAS_0	0	0	It sets the PLL buffer 2 bias from 0.8 mA (00) to 2 mA (11), 0.4-mA steps.
Bit17	RXBUF2_BIAS_1	1	1	
Bit18	RXBUFOUT_BIAS_0	0	0	RXPLL output-buffer reference bias current. 200 μA (00) to 500 μA (11)
Bit19	RXBUFOUT_BIAS_1	1	1	
Bit20	RXPRES_BIAS_0	1	0	RXPLL prescaler reference bias current. 200 μA (00) to 500 μA (11)
Bit21	RXPRES_BIAS_1	1	1	
Bit22	RXVCO_CAL_IB	0	1	Select bias-current type for VCO calibration circuitry; 1 = PTAT; 0 = constant over temperature
Bit23	RXVCO_CAL_REF_0	0	1	RX VCO calibration reference voltage trimming. 000 → 1.175 V 111 → 2.05 V. Suggested value is 1.55 V (011).
Bit24	RXVCO_CAL_REF_1	0	1	
Bit25	RXVCO_CAL_REF_2	0	0	
Bit26	RSV	0	0	Reserved
Bit27	RSV	0	0	Reserved
Bit28	RSV	0	0	Reserved
Bit29	RSV	0	0	Reserved
Bit30	RSV	0	0	Reserved
Bit31	RSV	0	0	Reserved

TX and RX SPI Registers

SPI3 Register 0

This is a read-only register, no write is possible. It contains the internal ADC 8-bit output.

Register address			SPI address		CONV DONE	OUT RANGE	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
RSV	RSV	RSV	RSV	RSV	RSV	TEMPOUT <7,0>								RSV	RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 0	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	0	0	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	0	0	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	CONVDONE	0	N/A	When 1, ADC conversion done
Bit6	OUTRANGE	0	N/A	When 1, the analog input voltage to the ADC falls outside the ADC input range of 0.125 V–1.125 V.
Bit7	RSV	0	N/A	Reserved
Bit8	RSV	0	N/A	Reserved
Bit9	RSV	0	N/A	Reserved
Bit10	RSV	0	N/A	Reserved
Bit11	RSV	0	N/A	Reserved
Bit12	RSV	0	N/A	Reserved
Bit13	RSV	0	N/A	Reserved
Bit14	RSV	0	N/A	Reserved
Bit15	RSV	0	N/A	Reserved
Bit16	RSV	0	N/A	Reserved
Bit17	RSV	0	N/A	Reserved
Bit18	RSV	0	N/A	Reserved
Bit19	RSV	0	N/A	Reserved
Bit20	RSV	0	N/A	Reserved
Bit21	RSV	0	N/A	Reserved
Bit22	TEMPOUT_0	0	N/A	ADC 8-bit output Input range 0.125 V to 1.125 V
Bit23	TEMPOUT_1	0	N/A	
Bit24	TEMPOUT_2	0	N/A	
Bit25	TEMPOUT_3	0	N/A	
Bit26	TEMPOUT_4	0	N/A	
Bit27	TEMPOUT_5	0	N/A	
Bit28	TEMPOUT_6	0	N/A	
Bit29	TEMPOUT_7	0	N/A	
Bit30	RSV	0	N/A	Reserved
Bit31	RSV	0	N/A	Reserved

SPI3 Register 1

Register address			SPI address		TX PWD	TX VGA attenuation control							TX I and Q phase unbalance correction		
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

TX I and ... correction		Enable loopback	Loopback attenuator	Detect reset	PD ref	RSV									
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 1	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	1	1	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	0	0	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	PWD_TX	1	0	TX chain power down (1 = TX chain is off)
Bit6	TX_ATT_0	0	App. specific	TX chain variable-attenuator control; 000 0000 = minimum attenuation; 100 0111 = maximum attenuation (35.5 dB); attenuation step = 0.5 dB;
Bit7	TX_ATT_1	0	App. specific	
Bit8	TX_ATT_2	0	App. specific	
Bit9	TX_ATT_3	1	App. specific	
Bit10	TX_ATT_4	0	App. specific	
Bit11	TX_ATT_5	0	App. specific	
Bit12	TX_ATT_6	0	App. specific	
Bit13	TXIQ_PHASE_0	0	0	TX LO I and Q phase-error correction bits. Suggested value is (0 1000).
Bit14	TXIQ_PHASE_1	0	0	
Bit15	TXIQ_PHASE_2	0	0	
Bit16	TXIQ_PHASE_3	0	1	
Bit17	TXIQ_PHASE_4	1	0	
Bit18	EN_LB	0	0	Enable loopback switch (1 = enable)
Bit19	EN_LB_ATT	0	0	Enable 20-dB attenuator in loopback (1 = enable)
Bit20	DET_RESET	0	0	Software reset of power-detect alarm output
Bit21	PD_REF_BUF	0	0	Power down reference-frequency input buffer (1 = disable)
Bit22	RSV	0	0	Reserved
Bit23	RSV	0	0	Reserved
Bit24	RSV	0	0	Reserved
Bit25	RSV	0	0	Reserved
Bit26	RSV	0	0	Reserved
Bit27	RSV	0	0	Reserved
Bit28	RSV	0	0	Reserved
Bit29	RSV	0	0	Reserved
Bit30	RSV	0	0	Reserved
Bit31	RSV	0	0	Reserved

PWD_TX (bit 5): When 1, the entire TX chain is off.

TX_ATT<6,0>: TX chain variable-attenuator control bits, 000 0000 corresponds to minimum attenuation (maximum gain), and 100 0111 sets the attenuator to maximum (minimum gain). The typical attenuation step is 0.5 dB.

TXIQ_PHASE<4,0>: TX I-Q phase unbalance correction bits. These bits allow correcting ±2 degrees of phase unbalance between the I and Q paths. Suggested value to program = 0 1000.

EN_LB (bit 18): When 1, the loopback switch, connecting the TX mixer output to the RX IFVGA3 input, is on. Also, when the switch is enabled, the TX amplifier, RX LNA, IFVGA1, and IFVGA2 are turned off (see the *Application Information* section).

EN_LB_ATT (bit 19): When 1, a 20-dB attenuator in the loopback path is enabled (see the *Application Information* section).

DET_RESET (bit 20): Set this bit to 1 to reset the power-alarm output after it has gone low for a power-alarm alert (see the *Application Information* section).

SPI3 Register 2

Register address			SPI address		RX LNA gain control					Enable ext SAW	RX baseband gain				
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

RX baseband-filter corner frequency							Filter bypass	Baseband 3-dB attenuation	PWD RX	PWD XPIC	XPIC baseband gain				
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 2	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	0	0	Register address bits
Bit1	ADDR_1	1	1	
Bit2	ADDR_2	0	0	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	LNA_ATT_0	0	App. specific	RX LNA attenuation control bits <0 0000> corresponds to 0-dB attenuation (maximum gain). <1 0011> corresponds to 19-dB attenuation (minimum gain). Gain step is 1 dB.
Bit6	LNA_ATT_1	0	App. specific	
Bit7	LNA_ATT_2	0	App. specific	
Bit8	LNA_ATT_3	0	App. specific	
Bit9	LNA_ATT_4	0	App. specific	
Bit10	EN_SAW	0	App. specific	1 = signal path through external SAW filter enabled
Bit11	RXBB_GAIN_0	0	App. specific	RX baseband amplifier gain setting <1 1000> = maximum gain (33 dB); gain step is 1 dB. RXBB_GAIN<4,0> = wanted gain – 9 Example: wanted gain = 22 dB → New gain setting = 22 – 9 = 13 = <0 1101>
Bit12	RXBB_GAIN_1	0	App. specific	
Bit13	RXBB_GAIN_2	0	App. specific	
Bit14	RXBB_GAIN_3	0	App. specific	
Bit15	RXBB_GAIN_4	1	App. specific	
Bit16	RXBB_FREQ_0	0	App. specific	RX baseband-filter cutoff-frequency setting Setting of <111 1111> corresponds to minimum cutoff frequency. See the *Baseband-Filter Cutoff-Frequency Calibration* section.
Bit17	RXBB_FREQ_1	1	App. specific	
Bit18	RXBB_FREQ_2	1	App. specific	
Bit19	RXBB_FREQ_3	1	App. specific	
Bit20	RXBB_FREQ_4	1	App. specific	
Bit21	RXBB_FREQ_5	0	App. specific	
Bit22	RXBB_FREQ_6	1	App. specific	
Bit23	RXBB_FLT_BYP	0	App. specific	RX baseband filter bypass
Bit24	RXBB_3dBATT	1	App. specific	Enable 3-dB attenuator in the RX BB output buffer (1 = on)
Bit25	PWD_RX	0	0	Power down receiver chain
Bit26	PWD_XPIC	0	0	Power down XPIC
Bit27	XPICBB_GAIN_0	0	App. specific	XPIC baseband-amplifier gain setting. <xxx> = maximum gain (xx dB); gain step is 1 dB. XPICBB_GAIN<4,0> = wanted gain – 9 Example: wanted gain = 12 dB → New gain setting = 12 – 9 = 3 = <0 0011>
Bit28	XPICBB_GAIN_1	1	App. specific	
Bit29	XPICBB_GAIN_2	1	App. specific	
Bit30	XPICBB_GAIN_3	0	App. specific	
Bit31	XPICBB_GAIN_4	0	App. specific	

LNA_ATT<4,0>: RX LNA attenuation setting. The LNA has 19 dB of gain range in 1-dB steps, as shown in Table 6.

Table 6. LNA Attenuation and Gain vs LNA_ATT<4,0>

LNA_ATT<4,0>	LNA ATTENUATION (dB)	LNA GAIN (dB)
<0 0000>	0	17
<00001>	1	16
<0 0010>	2	15
<0 0011>	3	14
<0 0100>	4	13
<0 0101>	5	12
<0 0110>	6	11
<0 0111>	7	10
<0 1000>	8	9
<0 1001>	9	8
<0 1010>	10	7
<0 1011>	11	6
<0 1100>	12	5
<0 1101>	13	4
<0 1110>	14	3
<0 1111>	15	2
<1 0000>	16	1
<1 0001>	17	0
<1 0010>	18	–1
<1 0011>	19	–2

EN_SAW (bit 10): It enables the external IF path (through the SAW filter) for the signal. When it is 1, the IFVGA1 output buffer (pins 2 and 3) and IFVGA2 input buffer (pins 62 and 63) are on, and the internal connection between the two VGAs is off (see Figure 101).

RXBB_GAIN<4,0>: RX baseband-amplifier gain setting. There are 25 gain settings (0 to 24) in 1-dB increments. <1 1000> = maximum gain (33 dB). To set a new gain, the following formula can be used:

gain_setting = wanted_gain – 9.

Example: Wanted gain = 22 dB → New gain setting = 22 – 9 = 13 = <0 1101>

RXBB_FREQ<6,0>: RX baseband-filter cutoff-frequency control. All 1s sets the filter to its minimum pass band; whereas all 0s sets the filter to its maximum cutoff frequency.

PWD_RX (bit 25): When it is 1, the entire RX chain is off.

PWD_XPIC (bit 26): When it is 1, XPIC (RX chain and output amplifier) is off.

XPICBB_GAIN<4,0>: XPIC baseband-amplifier gain setting. There are 13 gain settings (0 to 12) in 1-dB increments; <0 0000> = minimum gain (9 dB) and <0 1100> = maximum gain (21 dB). To set a new gain, the following formula can be used:

gain_setting = wanted_gain – 9.

Example: Wanted gain = 12 dB → New gain setting = 12 – 9 = 3 = <0 0011>

SPI3 Register 3

Register address			SPI address		Reserved				TX shut-down Time const		RSV	TXBIAS	TX VATT bias control		
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

TXLO IQ FLIP	TX mixer bias control		TX input dc-offset control: Q channel						TX input dc-offset control: I channel						EN TXBB bias
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 3	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	1	1	Register address bits
Bit1	ADDR_1	1	1	
Bit2	ADDR_2	0	0	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	RSV	0	0	Reserved
Bit6	RSV	0	0	Reserved
Bit7	RSV	0	0	Reserved
Bit8	RSV	0	0	Reserved
Bit9	PS_TC_0	0	App. specific	TX power-shutdown time constant: 00 = 28 µs; 01 = 42 µs; 10 = 57 µs; 11 = 75 µs
Bit10	PS_TC_1	0	App. specific	
Bit11	RSV	1	1	Reserved
Bit12	TXBETABIAS	0	0	TXAMP bias control (0 = low; 1 = high)
Bit13	TXATTBIAS_0	0	0	TX variable attenuator bias current control
Bit14	TXATTBIAS_1	0	0	
Bit15	TXATTBIAS_2	1	1	
Bit16	TX_IQ_SEL	0	0	Flip TX I with Q side
Bit17	TXMIXBIAS_0	0	0	TX mixer bias control
Bit18	TXMIXBIAS_1	1	1	
Bit19	TXBBQ_0	0	0	TX input baseband dc offset control: Q channel See the application note (SLWU064) for optimum dc-offset control setting.
Bit20	TXBBQ_1	0	0	
Bit21	TXBBQ_2	0	0	
Bit22	TXBBQ_3	0	0	
Bit23	TXBBQ_4	0	0	
Bit24	TXBBQ_5	1	1	
Bit25	TXBBI_0	0	0	TX input baseband dc-offset control: I channel See the application note (SLWU064) for optimum dc-offset control setting.
Bit26	TXBBI_1	0	0	
Bit27	TXBBI_2	0	0	
Bit28	TXBBI_3	0	0	
Bit29	TXBBI_4	0	0	
Bit30	TXBBI_5	1	1	
Bit31	EN_TXCM	0	0	Enable external TX baseband common-mode generation (0 = internal common-mode voltage generation; 1 = external common-mode voltage generation)

PS_TC<1,0>: TX power-shutdown time constant. It controls how fast the TX output power is ramped down after TXPWD (pin 17) is set high. The typical shutdown time (output level attenuated by 30 dB) is shown in Table 7.

Table 7. TX Power Shutdown Time vs PS_TC<1,0>

PS_TC	POWER DOWN
00	28 μs
01	42 μs
10	57 μs
11	75 μs

TXBBQ<4,0> and TXBBI<4,0>: TX input baseband dc-offset control bits. Suggested value is <1 0000>, that corresponds to 0-V applied offset.

EN_TXCM: When 1, the TX baseband input common mode is generated internally.

SPI3 Register 4

Register address			SPI address		EN TEMP ADC cal	XPIC AMP bias sel	XPIC AMP bias control		XPIC AMP gain control			RX VGA bias control ..			
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

..	PWD TX chain blocks				PWD T_ADC	PWD T_SENS	PWD RX and XPIC blocks								RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 4	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	0	0	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	1	1	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	EN_TADC_CAL	0	0	Enable temperature-sensor ADC calibration
Bit6	XPICAMPBIAS_SEL	0	0	Select bias type (1 = PTAT; 0 = CONST)
Bit7	XPICAMPBIAS_0	0	0	XPIC output-amplifier bias control
Bit8	XPICAMPBIAS_1	1	1	
Bit9	XPICAMPGAIN_0	0	0	XPIC output-amplifier gain adjustment
Bit10	XPICAMPGAIN_1	0	1	
Bit11	XPICAMPGAIN_2	1	0	
Bit12	RXVGABIAS_0	1	1	RX VGAs bias control
Bit13	RXVGABIAS_1	0	1	
Bit14	RXVGABIAS_2	0	1	
Bit15	RXVGABIAS_3	1	0	
Bit16	RXVGABIAS_4	0	0	
Bit17	PWD_TXMIX	0	0	Power down TX modulator (1 = disable)
Bit18	PWD_TXATT	0	0	Power down TX variable attenuator (1 = disable)
Bit19	PWD_TXPREAMP	0	0	Power down TX amplifier driver (1 = disable)
Bit20	PWD_TXAMP	0	0	Power down TX output amplifier (1 = disable)
Bit21	PWD_TEMPADC	1	1	Power down TEMP sensor ADC (1 = disable)
Bit22	PWD_TEMPSENS	1	1	Power down TEMP sensor (1 = disable)
Bit23	PWD_DCOFF	0	0	Power down RX dc offset loop (1 = disable)
Bit24	PWD_XPICAMP	0	0	Power down XPIC output amplifier (1 = disable)
Bit25	PWD_LNA	0	0	Power down RX LNA (1 = disable)
Bit26	PWD_IFVGA1	0	0	Power down RX IFVGA1 (1 = disable)
Bit27	PWD_IFVGA2	0	0	Power down RX IFVGA2 (1 = disable)

REGISTER 4	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit28	PWD_IFVGA3	0	0	Power down RX IFVGA3 (1 = disable)
Bit29	PWD_RXMIX	0	0	Power down RX demodulator (1 = disable)
Bit30	PWD_RXBB	0	0	Power down RX baseband (1 = disable)
Bit31	RSV	0	0	Reserved

EN_TADC_CAL (bit 5): When 1, TEMP sensor ADC autocalibration starts.

XPICAMPBIAS_SEL (bit 6): It selects the XPIC output amplifier biasing type. When 1, a PTAT (proportional to temperature) dc current is selected. If it is 0, then a constant current over temperature is chosen.

SPI3 Register 5

Register address			SPI address		ENBB AUTOCAL	RXMIX BIAS		RX IMIX VCM		RXQMIX VCM		DC offset resolution		DC offset CLK	
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

...	RSV	ENXPIC CAL	XPIC MIX BIAS		XPIC IMIX VCM		XPIC QMIX VCM		XPIC dc offset resolution		XPIC dc offset CLK			RSV	PWD dc OFF
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 5	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	1	1	Register address bits
Bit1	ADDR_1	0	0	
Bit2	ADDR_2	1	1	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	EN_BB_AUTOCAL	0	0	Enable RX baseband dc-offset autocalibration
Bit6	RXMIX_BIAS_0	1	1	RX demodulator dc current control
Bit7	RXMIX_BIAS_1	0	0	
Bit8	RXIMIX_VCM_0	0	0	RX I mixer bias control
Bit9	RXIMIX_VCM_1	1	1	
Bit10	RXQMIX_VCM_0	0	0	RX Q mixer bias control
Bit11	RXQMIX_VCM_1	1	1	
Bit12	DCOFF_BIAS_0	1	1	Set RX dc-offset calibration-loop resolution
Bit13	DCOFF_BIAS_1	1	1	
Bit14	DCOFF_CLK_0	0	0	RX dc offset-loop clock-speed control
Bit15	DCOFF_CLK_1	0	0	
Bit16	DCOFF_CLK_2	1	1	
Bit17	RSV	0	0	Reserved
Bit18	EN_XPIC_AUTOCAL	0	0	Enable XPIC baseband dc-offset autocalibration
Bit19	XMIX_BIAS_0	1	0	XPIC demodulator dc-current control
Bit20	XMIX_BIAS_1	0	1	
Bit21	XIMIX_VCM_0	0	0	XPIC I mixer bias control
Bit22	XIMIX_VCM_1	1	1	
Bit23	XQMIX_VCM_0	0	0	XPIC Q mixer bias control
Bit24	XQMIX_VCM_1	1	1	
Bit25	XPICDCOFF_BIAS_0	1	1	Set XPIC dc-offset calibration-loop resolution
Bit26	XPICDCOFF_BIAS_1	1	1	
Bit27	XDCOFF_CLK_0	0	0	XPIC dc offset-loop clock-speed control
Bit28	XDCOFF_CLK_1	0	0	
Bit29	XDCOFF_CLK_2	1	1	
Bit30	RSV	1	1	Reserved

REGISTER 5	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit31	PWD_XPICDCOFF	0	0	Power down XPIC dc-offset loop (1 = disable)

EN_BB_AUTOCAL (bit5): When 1, the RX baseband dc-offset automatic calibration starts. At the end of the calibration, the bit is reset to 0.

DCOFF_BIAS<2,0>: These bits control the maximum output dc voltage of the dc-offset correction DAC used in the RX chain.

DCOFF_CLK<2,0>: It sets the frequency-divider ratio that creates the RX dc-offset correction-loop clock from the clock divider.

EN_BB_CAL (bit17): When 1, the RX baseband dc-offset loop is enabled.

EN_XPIC_AUTOCAL (bit18): When 1, the XPIC baseband dc-offset automatic calibration starts. At the end of the calibration, the bit is reset to 0.

XPICDCOFF_BIAS<2,0>: These bits control the maximum output dc voltage of the dc-offset correction DAC used in the XPIC chain.

XDCOFF_CLK<2,0>: It sets the frequency-divider ratio that creates the XPIC dc-offset correction-loop clock from the clock divider.

SPI3 Register 6

Register address			SPI address		IFVGA3 gain-range control					IFVGA3 min. gain				IFVGA2 gain-range control	
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

IFVGA2 gain-range control			IFVGA2 min. gain				IFVGA1 gain-range control					IFVGA1 min. gain			
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 6	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	0	0	Register address bits
Bit1	ADDR_1	1	1	
Bit2	ADDR_2	1	1	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	IFVGA3_RANGE_0	0	0	IFVGA3 gain-range control
Bit6	IFVGA3_RANGE_1	0	1	
Bit7	IFVGA3_RANGE_2	1	0	
Bit8	IFVGA3_RANGE_3	1	1	
Bit9	IFVGA3_RANGE_4	1	0	
Bit10	IFVGA3_ MINGAIN_0	0	0	IFVGA3 minimum-gain control
Bit11	IFVGA3_MINGAIN_1	1	1	
Bit12	IFVGA3_MINGAIN_2	0	0	
Bit13	IFVGA3_MINGAIN_3	0	0	
Bit14	IFVGA2_RANGE_0	0	1	IFVGA2 gain-range control
Bit15	IFVGA2_RANGE_1	0	0	
Bit16	IFVGA2_RANGE_2	1	0	
Bit17	IFVGA2_RANGE_3	1	1	
Bit18	IFVGA2_RANGE_4	1	0	
Bit19	IFVGA2_ MINGAIN_0	0	0	IFVGA2 minimum-gain control
Bit20	IFVGA2_MINGAIN_1	1	1	
Bit21	IFVGA2_MINGAIN_2	0	0	
Bit22	IFVGA2_MINGAIN_3	0	0	

REGISTER 6	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit23	IFVGA1_RANGE_0	0	0	IFVGA1 gain-range control
Bit24	IFVGA1_RANGE_1	0	0	
Bit25	IFVGA1_RANGE_2	1	1	
Bit26	IFVGA1_RANGE_3	1	1	
Bit27	IFVGA1_RANGE_4	1	1	
Bit28	IFVGA1_ MINGAIN_0	0	0	IFVGA1 minimum-gain control
Bit29	IFVGA1_MINGAIN_1	1	0	
Bit30	IFVGA1_MINGAIN_2	0	1	
Bit31	IFVGA1_MINGAIN_3	0	0	

SPI3 Register 7

Register address			SPI address		RX BB I dc offset DAC								RX BB Q dc offset DAC		
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

RX BB Q dc offset DAC					CAL SEL	PWD DET DELAY		PWR DETECTOR THRESHOLD			RSV	RSV	RSV	RSV	RSV
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

REGISTER 7	NAME	POWER-ON VALUE	SUGGESTED VALUE	DESCRIPTION
Bit0	ADDR_0	1	1	Register address bits
Bit1	ADDR_1	1	1	
Bit2	ADDR_2	1	1	
Bit3	ADDR_3	1	1	SPI address bits
Bit4	ADDR_4	1	1	
Bit5	RXBBI_DCOFF_0	0	0	RX baseband I-side dc-offset control DAC
Bit6	RXBBI_DCOFF_1	0	0	
Bit7	RXBBI_DCOFF_2	0	0	
Bit8	RXBBI_DCOFF_3	0	0	
Bit9	RXBBI_DCOFF_4	0	0	
Bit10	RXBBI_DCOFF_5	0	0	
Bit11	RXBBI_DCOFF_6	0	0	
Bit12	RXBBI_DCOFF_7	1	1	
Bit13	RXBBQ_DCOFF_0	0	0	RX baseband Q-side dc-offset control DAC
Bit14	RXBBQ_DCOFF_1	0	0	
Bit15	RXBBQ_DCOFF_2	0	0	
Bit16	RXBBQ_DCOFF_3	0	0	
Bit17	RXBBQ_DCOFF_4	0	0	
Bit18	RXBBQ_DCOFF_5	0	0	
Bit19	RXBBQ_DCOFF_6	0	0	
Bit20	RXBBQ_DCOFF_7	1	1	
Bit21	RXBB_CALSELECT	1	1	RX baseband dc-offset calibration select (1 = automatic; 0 = manual)
Bit22	PWRDET_DEL_0	1	App. Specific	Power-detector-response delay control
Bit23	PWRDET_DEL_1	0	App. Specific	
Bit25	PWRDET_0	0	0	TX power-detector threshold setting
Bit25	PWRDET_1	0	1	
Bit26	PWRDET_2	0	0	
Bit27	RSV	0	0	Reserved
Bit28	RSV	0	0	Reserved
Bit29	RSV	0	0	Reserved
Bit30	RSV	0	0	Reserved
Bit31	RSV	0	0	Reserved

RXBBI_DCOFF<7,0> and RXBBI_DCOFF<7,0>: TRF2443 internal auxiliary DAC bits to be set during the manual RX-chain baseband dc-offset calibration (see the *Application Information* section).

RXBB_CALSELECT (bit 21): Selects the dc-offset calibration mode; when 0, the manual mode is selected.

PWRDET_DEL<1,0>: TX power-detector response-time delay (see Table 8).

Table 8. TX Power-Detector Response-Time Delay vs PWRDET_DEL<1,0>

PWRDET_DEL	DET DELAY
00	5 µs
01	10 µs
10	20 µs
11	40 µs

PWRDET<2,0>: TX power-detector threshold-level control

READBACK MODE

The TRF2443 implements the capability to read back the content of the serial programming-interface registers. Each readback is composed of two phases:

1. Writing a request to read back data
2. Reading the actual data of the internal registers (see timing diagram in Figure 100).

During the writing phase, a command is sent to the TRF2443 to set it in readback mode and to specify which register is to be read. In the proper reading phase, at each rising clock edge, the internal data is transferred to the RDBKSPI pin and can be read at the following falling edge (LSB first). The first clock after the LE goes high (end of writing cycle) is idle, and the following 32 clock pulses transfer the internal register content to the RDBKSPI pin.

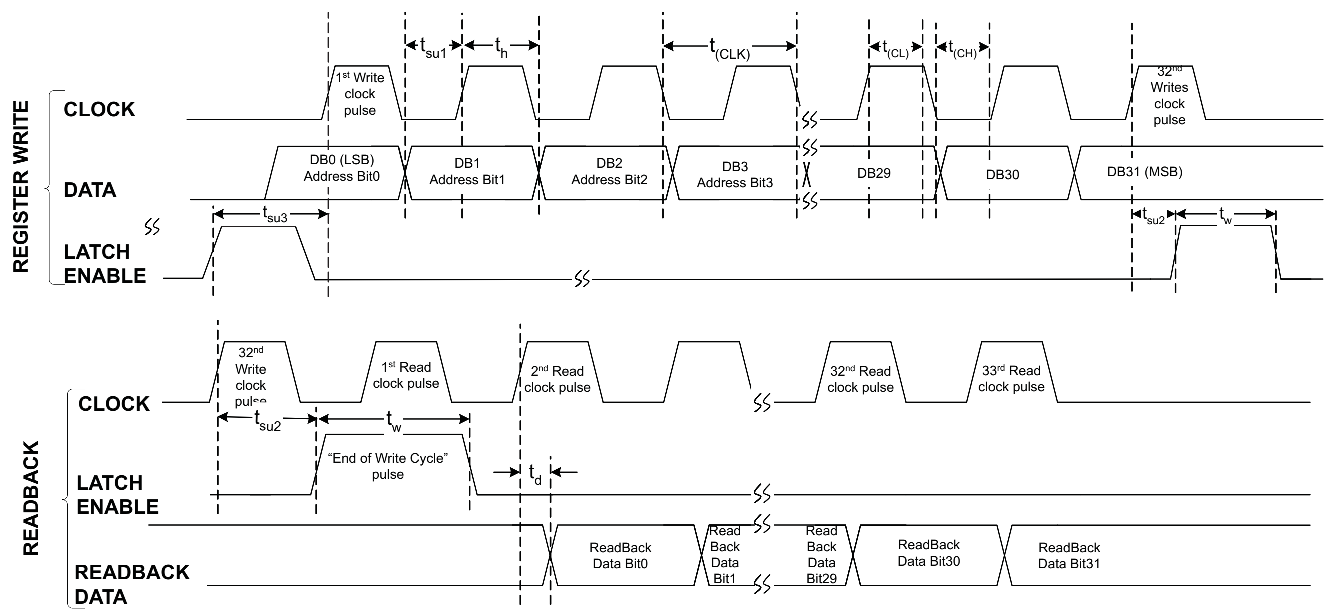


Figure 100. SPI Readback Timing Diagram

Table 9. SPI Readback Timing

PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
t_h	Hold time, data to clock	20			ns	
t_{SU1}	Setup time, data to clock	20			ns	
$t_{(CL)}$	Clock low duration	20			ns	
$t_{(CH)}$	Clock high duration	20			ns	
t_{SU2}	Setup time, clock to enable	20			ns	
t_W	Enable time	50			ns	Equals clock period
$t_{(CLK)}$	Clock period	50			ns	
t_{SU3}	Setup time, latch to data	70			ns	
t_d	Delay time, clock to readback-data output	10			ns	

Readback From the Internal Register Banks

The TX PLL (SPI-1) and RX PLL (SPI-2) register banks each contain six registers: register 0 (000) through register 5 (101). Register 0 (000) is used only for the readback operation, whereas registers 1 through 5 are the actual PLL control registers. In the case of the TX PLL (SPI-1) and RX PLL (SPI-2) register banks, register 0 contains no information. Therefore, it is not possible to read back register 0 from these register banks.

The TX-RX (SPI-3) register bank contains eight registers: register 0 (000) through register 7 (111). Register 0 (000) is used only for the readback operation, whereas registers 1 through 7 are the actual TX and RX control registers. In the case of the TX-RX register bank (SPI-3), register 0 is used to store some TRF2443 internal data. Therefore, it is possible to read back register 0 from this register bank, as it contains this data.

To read back a register from any of these register banks, register 0 of the register bank which contains the register to be read must be programmed with a specific command that sets the TRF2443 in the readback mode and specifies the register to be read:

- Set B<31> to 1 to put the TRF2443 in readback mode.
- Set B<30,28> equal to the address of the register to be read (001 to 101 in the case of TX PLL/RX PLL; 000 to 111 in the case of TX-RX SPI).

Table 10. SPI Register Banks Readback Setup

BITS		NAME	SUGGESTED VALUE	DESCRIPTION
Address bits	B0	ADDR <0>	0	Register 0 to be programmed to set TRF2443 in readback mode
	B1	ADDR <1>	0	
	B2	ADDR <2>	0	
	B3	ADDR <3>	X	Register bank: B<4,3> from which a particular register is to be read back TX PLL (01); RX PLL (10); TX-RX SPI (11)
	B4	ADDR <4>	X	
Data field	B5	N/C	0	
	B6	N/C	0	
	B7	N/C	0	
	B8	N/C	0	
	B9	N/C	0	
	B10	N/C	0	
	B11	N/C	0	
	B12	N/C	0	
	B13	N/C	0	
	B14	N/C	0	
	B15	N/C	0	
	B16	N/C	0	
	B17	N/C	0	
	B19	N/C	0	
	B20	N/C	0	
	B21	N/C	0	
	B22	N/C	0	
	B23	N/C	0	
	B24	N/C	0	
	B25	N/C	0	
	B26	N/C	0	
	B27	N/C	0	
	B28	RB_REG<0>	X	Address of the register within the bank that is being read back; Reg 1(001) to Reg 5(101) in TX PLL/RX PLL; Reg 0(000) to Reg 7(111) in TX-RX SPI
	B29	RB_REG<1>	X	
	B30	RB_REG<2>	X	
	B31	RB_Enable	1	1 → Put the device in readback mode

TRF2443 DESCRIPTION

RECEIVER DESCRIPTION

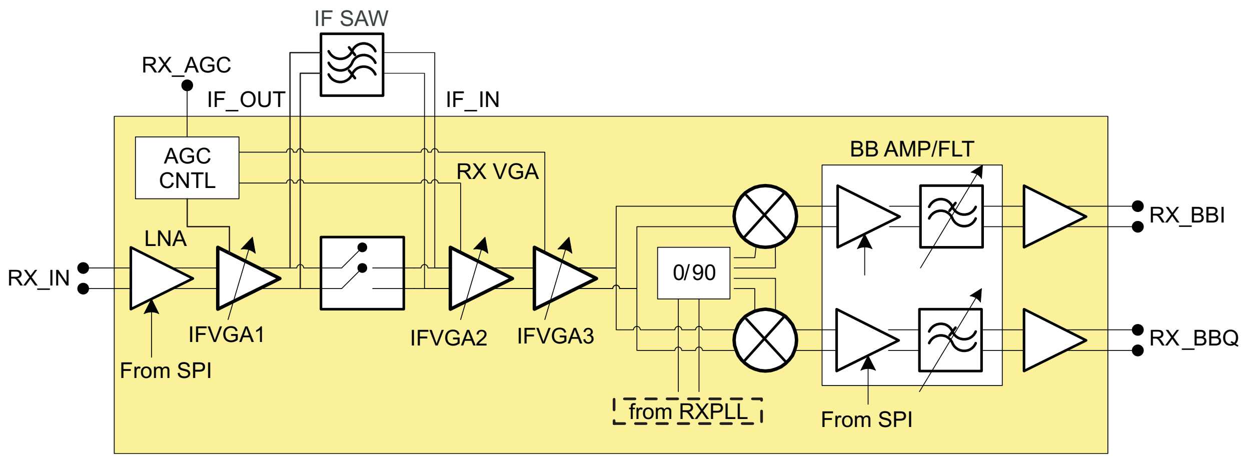


Figure 101. Receiver Chain Block Diagram

The TRF2443 features a highly linear low-noise receiver chain with over 60 dB of analog-controlled gain range and more than 40 dB of gain range programmable via the serial programming interface (SPI) in 1-dB steps. Moreover, the TRF2443 gives the flexibility to add an external IF filter to further remove unwanted signals. Such an external filter can be bypassed using an internal path that can be enabled via SPI.

LNA

The first block of the receiver chain is a low-noise, highly linear IF amplifier (LNA). Its input is differential and internally matched to 50 Ω. To drive the TRF2443 RX input via a single0-ended source, a 1:1 balun is required at the LNA input (see *Application Schematic* section). The TRF2443 LNA attenuation is programmable via the serial programming interface (SPI) from 0 dB to –19 dB, corresponding to an LNA gain of 17 dB to –2 dB (1-dB steps). LNA_ATT<4,0> in SPI-3, register 2, B<9,5> are the LNA attenuation controlling bits. To program the amplifier to the maximum gain, set the attenuation bits to 0 (LNA_ATT<4,0> = <0 0000>); whereas minimum gain corresponds to LNA_ATT<4,0> = <1 0011>.

VGA

The LNA is followed by three analog-controlled VGAs that provide more than 60 dB of gain range. The IFVGA1 output and IFVGA2 input can be connected externally (pins IFOUT and IFIN) through an external IF filter. The IFVGA1 output buffer requires two pullup inductors to be connected from the IFOUTP/N pins to Vcc (see *Application Schematic* section). The IFVGA2 input (pins IFINN/P) is high-impedance. A 50-Ω external resistor is required across the IFINN and IFINP pins to provide a matching load to the IF filter output. An internal switch gives the flexibility to bypass the external filter. The internal bypass switch is controlled via the serial programming interface through bit EN_SAW (SPI-3, register 2, B<10>). By programming EN_SAW to 1, the external path is selected, whereas a 0 engages the internal bypass switch.

The VGA gain is controlled by the dc voltage applied to the RXAGC pin. By varying the input dc voltage from 0 V to 2 V, the VGA total gain goes from minimum to maximum. The gain control is linear in dB, with a typical slope around 51 dB/V. The RXAGC input provides a high input impedance, equivalent to a 100-kΩ resistance in series with a 4-pF capacitance.

Demodulator

The IFVGA3 drives the demodulator, which downconverts the IF input signal directly to baseband in phase and quadrature. The demodulator block includes the local oscillator in-phase and quadrature-generation circuitry, followed by the LO buffer. The LO chain also includes a frequency divider that can be programmed to divide by 8 or 16. The frequency divider generates the RX LO from the RX VCO. By selecting a division ratio of 16, the RX LO can be set to 140 MHz (see the *Programming the TRF2443 Synthesizers* section).

Baseband Section

The TRF2443 baseband section integrates a programmable gain amplifier (PGA) and programmable low-pass filter. The baseband PGA minimum gain is 9 dB, and the maximum gain is 33 dB. The PGA can be programmed in 25 gain settings (0 to 24) in 1-dB increments. Its gain can be changed by the RX_BBGAIN<4,0> bits (SPI-3, register 2, B<15,11> according to the following formula:

gain_setting = wanted_gain – 9.

Example: Wanted gain = 22 dB → New gain setting = 22 – 9 = 13 = <0 1101>

The TRF2443 baseband low-pass filter cutoff frequency can be programmed from 2 MHz to 11 MHz by setting appropriately the cutoff-frequency control bits RXBB_FREQ<6,0> (SPI-3, register 2, B<22,16>). RXBB_FREQ<6,0> = <111 1111> corresponds to the minimum corner frequency.

The baseband output buffers (ADC drivers) are designed to drive directly an analog-to-digital converter (ADC), either dc- or ac-coupled. The output common mode of the ADC drivers is set externally via the RXBBCM pin (pin 40). When the TRF2443 is dc-connected to the ADC, the same dc common mode for both the ADC and the TRF2443 baseband output can be used.

TRANSMITTER DESCRIPTION

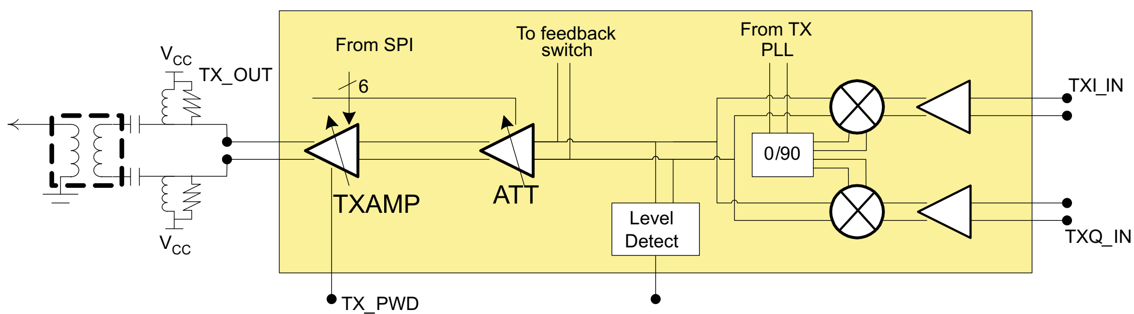


Figure 102. Transmitter Chain Block Diagram

The transmitter chain integrates an IQ modulator followed by a variable attenuator and the final transmitter amplification stage. The last two blocks provide over 35 dB of gain range. A power-alarm circuit monitors the level at the modulator output, and its digital output goes low if the signal level falls below the user-specified threshold level relative to the expected level.

TX IQ Modulator

The first block of the transmitter chain is the IQ modulator, which upconverts the incoming in-phase and quadrature signals to the TX IF frequency. The TRF2443 can be either ac- or dc-coupled to the digital-to-analog converter (DAC). If a dc-coupled configuration is selected, then the modulator-input dc-common mode must be set externally to the appropriate level of 1.4 V and the common-mode bias generation must be set to external mode via the SPI by setting EN_TXCM (SPI-3, register 3, B<31>) to 1. If an ac-coupled configuration is selected, then internal common-mode generation mode must be enabled via the SPI by setting EN_TXCM (SPI-3, register 3, B<31>) to 0. When internal biasing is enabled, it is possible to apply a dc offset to either the I or Q side of the IQ modulator using the integrated dc DAC, accessible via the SPI (TXBBI<5,0>, SPI-3, register 3, B<30,25>; TXBBQ<5,0>, SPI-3, register 3, B<24,19>). An external 100 Ω differential resistor is required between the TX baseband input pins (TXBBIP and TXBBIN, pins 22 and 21, and TXBBQP and TXBBQN, pins 20 and 19) if utilizing the dc DAC. The optimum value of the dc DAC, which minimizes carrier leakage, can be read from the EEPROM within the TRF2443. See the application note (SLWU064) on how to access EEPROM information. The mixers of the IQ modulator use an external load. The collectors of the output transistors are connected to the pins MIXINDN and MIXINDP (pins 2 and 3). On the board, a pullup inductor to Vcc must be connected to each of those pins, as well as a shunt resistor between the pins (see the *Application Schematic* section).

TX Variable Attenuator and Output Amplifier

The IQ modulator drives a variable attenuator. This block provides 5.5 dB of total attenuation range in 0.5-dB steps. The output amplifier integrates five attenuation steps of 6 dB each for total of 30 dB. The output amplifier in combination with the variable attenuator provides over 35.5 dB of monotonic output power control (0.5-dB steps). The TRF2443 TX gain can be controlled via SPI TX_ATT<6,0> (SPI-3, register 1, B<12,6>). TX_ATT<6,0> sets the amount of attenuation in the variable attenuator and output amplifier.

- TX_ATT<6,0> = 000 0000 → 0 dB attenuation (maximum gain)
- TX_ATT<6,0> = 100 0111 → maximum attenuation (minimum gain)

The TX output amplifier uses an output open-collector arrangement. Therefore, each of the two output pins (TXOUTP and TXOUTN, pins 77 and 78) requires a pullup inductor connected to the power supply (see the *Application Schematic* section). The TRF2443 TX output impedance is set typically to 200 Ω differential. A 4:1 impedance-ratio balun is needed to transform the impedance to 50 Ω single-ended.

SYNTHESIZERS DESCRIPTION

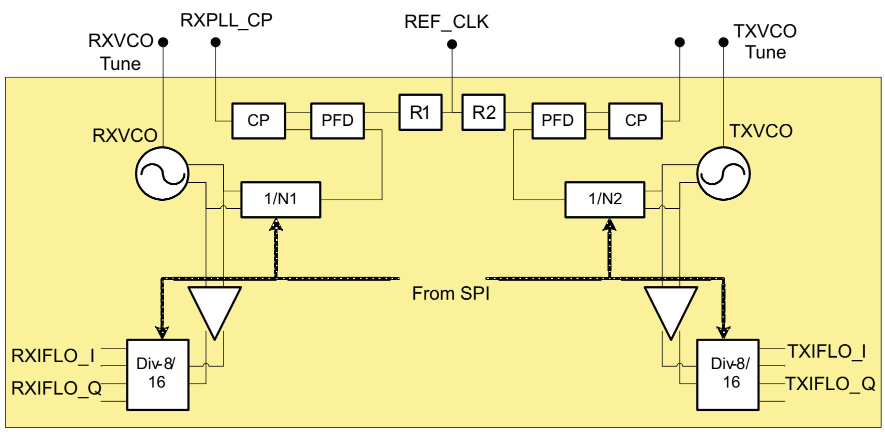


Figure 103. RX and TX PLL Block Diagram

The TRF2443 integrates two complete integer synthesizers for the receiver and transmitter chains. The RXVCO operates at 16 times the typical RX input frequency, and the TXVCO operates at 8 times the typical TX output frequency.

Each synthesizer is composed of:

- High-frequency VCO (around 2720 MHz for the TX VCO and 2240 MHz for the RX VCO)
- N-divider (driven by the high-frequency VCO) done by an 8/9 prescaler followed by an A-B counter that drives the phase-frequency detector
- Phase-frequency detector (PFD) (driven by the N-divider) that compares the VCO divided by N to the reference clock divided by R signals
- Charge pump (driven by the PFD), which creates up and down current pulses based on the incoming signals from the PFD. Its output is filtered and transformed to voltage by the external loop filter and applied to the VCO input control voltage.
- An external reference clock must be applied to REFIN (pin 16). The incoming signal is buffered and goes through a programmable divider (R-divider).

The VCO output is then routed through a programmable divider by 8 or 16 to create the TX and RX LO signals. The TRF2443 features a lock-detect output pin (LOCKDET, pin 5). This is a digital output that is high when both RX and TX synthesizers are locked, and it is low if one or both synthesizers are unlocked (or lose lock).

Programming the TRF2443 Synthesizers

Both TRF2443 synthesizers are integer PLLs. The VCO output frequency is defined by:

$f_{VCO} = k \times N / R \times f_{Ref}$

where:

N: division ratio of the N-divider
R: division ratio of the R-divider
K: multiplier factor; k = 1 for RX synthesizer; k = 2 for the TX synthesizer.

Knowing the f_{Ref}, it is possible to calculate the required N and R values to synthesize any output frequency within the VCO frequency range.

Example

Suppose we want to synthesize the TX LO to be 340 MHz and the input reference frequency is 20 MHz.

LO_{TX} = 340 MHz
f_{Ref} = 20 MHz
$f_{VCO\text{-}TX}$ = 2720 MHz (8 × LO_{TX})

Because $f_{VCO\text{-}TX}$ is an integer multiple of f_{Ref}, we can set the R divider to 1.

R = 1
N = $f_{VCO\text{-}TX}$ / (k × f_{Ref}) × R = 68

Then the TRF2443 SPI can be programmed as follows:

R = 1 → TXRDIV<13,0> = <00 0000 0000 0001> (SPI-1, register 1, B<18,5>)
N = 68 → TX_NINT<15,0> = <0000 0000 0100 0100> (SPI-1, register 2, B<20,5>)
LO divider set to 8 → TXDIV_SEL = 1 (SPI-1, register 2, B<26>).

Calibrating TRF2443 TX and RX VCO

Both TRF2443 VCOs are based on a cross-coupled LC tank architecture. The tank is composed of a high-Q integrated spiral inductor, a varactor, and an array of capacitors which is digitally controlled. To tune the VCO to a certain frequency, the correct configuration for the array of capacitors is required. The capacitor array can be configured automatically or manually.

The calibration mode is controlled by TXCAL_SEL (SPI-1, register 2, B<30>) for the TX VCO and by RXCAL_SEL (SPI-2, register 2, B<30>) for the RX VCO. Setting these two bits to 1 selects the automatic calibration mode. The calibration starts when EN_TXCAL (SPI-1, register 2, B<31>) and/or EN_RXCAL (SPI-2, register 2, B<31>) are toggled to 1. The calibration speed is controlled by a clock derived from the reference clock through a frequency divider, whose division ratio can be programmed with TXCAL_CLK<2,0> (SPI-1, register 2, B<29,27>) and RXCAL_CLK<2,0> (SPI-2, register 2, B<29,27>). The suggested value of TXCAL_CLK<2,0> and RXCAL_CLK<2,0> = <101>, which corresponds to a divider value of 1024 and a clock speed of 20 MHz.

The manual-mode calibration, used mainly for debugging purposes, is activated by setting TXCAL_SEL (SPI-1, register 2, B<30>) and or RXCAL_SEL (SPI-2, register 2, B<30>) to 0. In this mode, the capacitor array setting is controlled by TXVCO_TRIM<5,0> (SPI-1, register 4, B<31,26>) for the TX VCO and RXVCO_TRIM<6,0> (SPI-2, register 4, B<31,26>) for the RX VCO.

Synthesizer Lock-Detector Indicator

The TRF2443 integrates a PLL lock-detector circuit. When both the TX and RX synthesizers are locked, LOCKDET (pin 5) goes high. The settling time of the lock-detector circuitry can be set externally by sizing the capacitor placed between LDCAP (pin 38) and ground. The size of capacitor on this pin sets the time constant Tld of the lock detect circuit. If either the TX PLL or the RX PLL lock-detect circuit indicates a loss of lock, the LOCKDET pin goes low immediately.

If the lock-detect circuits of the TX and the RX PLLs have not indicated a loss of lock for a time > Tld, the LOCKDET pin goes high. For a 20-MHz PFD frequency, a 1-nF capacitor is suggested, corresponding to a 10-µs deglitch time.

XPIC DESCRIPTION

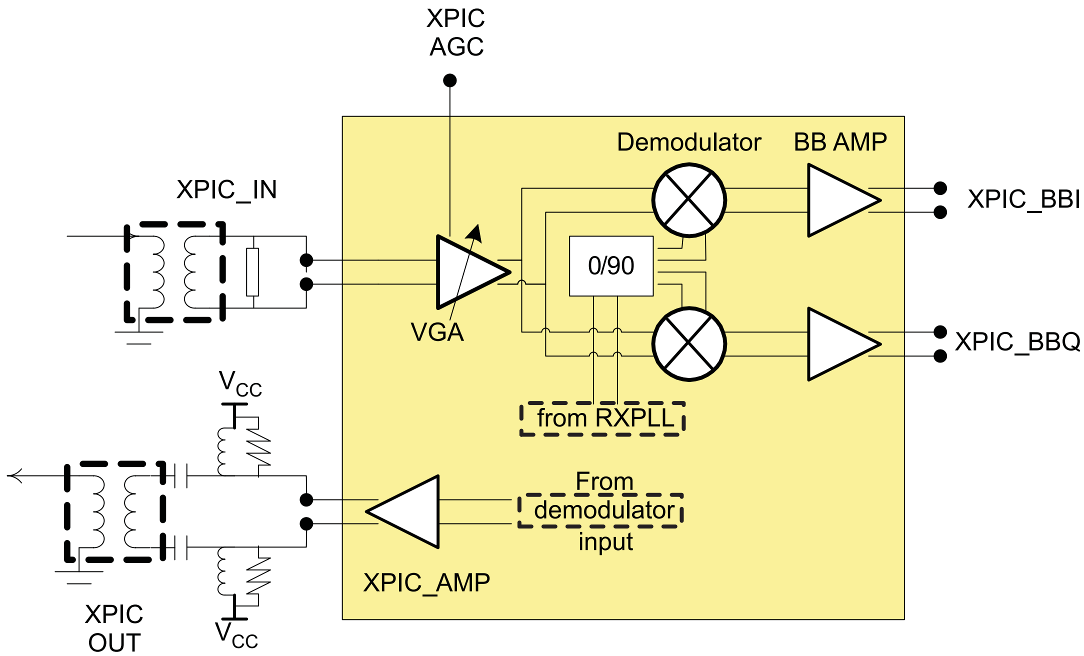


Figure 104. XPIC Block Diagram

XPIC Output Amplifier

The XPIC output amplifier transmits the signal taken at the receiver demodulator input. The XPIC output amplifier uses an output open-collector arrangement. Therefore, each of the output pins (XPICOUTN and XPICOUTP, pins 54 and 55) requires a pullup inductor to the power supply (see the *Application Schematic* section). The TRF2443 XPIC output impedance is set to 75 Ω differential with an internal resistor. A 1:1 impedance-ratio balun is needed to transform the impedance to 75 Ω single-ended.

XPIC Receiver Chain

The XPIC receiver section downconverts the input signal to baseband I and Q. It includes an IF VGA followed by a demodulator and a baseband amplifier. The XPIC receiver input is differential, but it can be converted to a single-ended 75-Ω input through an external 1:1 balun. The XPIC input impedance is set to 75 Ω with an internal resistor.

APPLICATION INFORMATION

POWER SUPPLY RAMP-UP PROCEDURE

In order to assure the correct functionality of the TRF2443 internal registers, it is important to ramp up the VCCREF power supply at the same time as or before VCCSPI. If VCCREF is powered before VCCSPI, the EEPROM contents could potentially be erased.

TRF2443 SPI INITIALIZATION SEQUENCE

In order to ensure proper operation of the TRF2443, it is important to program the IC through the SPI in a particular manner. How to do this is the scope of this section. The chip initialization can be broken down into four parts:

- Acquire information from EEPROM needed for subsequent initializations
- Initialize receiver PLL (SPI-2)
- Initialize transmitter PLL (SPI-1)
- Initialize receiver and transmitter (SPI-3)

EEPROM

There is information stored in the EEPROM that is available to the user to program the TRF2443 into an optimal state. If desired, the user must first read this information from the EEPROM and make it available for subsequent SPI programming. See the application note (SLWU064) on how to access EEPROM information.

Initialize RX PLL (SPI-2)

Write registers 4, 5, 1, and 2 of SPI-2 in this order. Register 2 is the last register to be written because register 2 starts the RX VCO calibration and PLL lock. The time required for this calibration to complete is 12 cycles of the *calibration frequency*. The calibration frequency is the external reference frequency divided by the RX_CAL CLK<2,0> (SPI-2, register 2, B<29,27>) setting. With a 20-MHz external reference and RX_CAL CLK<2,0> = <111> corresponding to a divider ratio of 16,684, this calibration frequency is 1.2 kHz. Therefore, the calibration requires 10 ms. The user should set the external reference frequency and the RX_CAL CLK<2,0> setting to ensure that the calibration frequency does not exceed 800 kHz. Subsequent register writes to SPI-1 and SPI-3 do not affect the RX VCO calibration and can begin immediately on the next SPI clock cycle.

Initialize TX PLL (SPI-1)

Write registers 4, 5, 1, and 2 of SPI-1 in this order. Register 2 is the last register to be written because register 2 starts the TX VCO calibration and PLL lock. The time required for this calibration to complete is 11 cycles of the *calibration frequency*. The calibration frequency is the external reference frequency divided by the TX_CAL CLK<2,0> (SPI-1, register 2, B<29,27>) setting. With a 20-MHz external reference and TX_CAL CLK<2,0> = <111>, corresponding to a divider ratio of 16,684, this calibration frequency is 1.2 kHz. Therefore, this calibration requires 9.2 ms. The user should set the external reference frequency and the TX_CAL CLK<2,0> setting to ensure that the calibration frequency does not exceed 800 kHz. Subsequent register writes to SPI-3 do not affect the TX VCO calibration and can begin immediately on the next SPI clock cycle.

Initialize RX and TX

Write registers 6, 3, 7, 4, 2, 5, 1, and 1 again of SPI-3 in this order. Register 5 starts the RX dc offset calibration. Register 1 follows register 5 and can be written immediately on the next SPI clock cycle, because its content does not affect the RX dc-offset calibration. Register 1 is written last because it contains the PWD_TX bit (SPI-3, register 1, B<5>). This ensures that all the other parameters of the TX are set up correctly before the transmitter is enabled. However, the power alarm circuitry (See the *Power Alarm Detector* section) is reset from register 1 by DET_RESET (SPI-3, register 1, B<20>). Because the TX is enabled at the same time the power alarm circuitry is reset, there exists a race condition which could cause the power alarm to be in either state. To ensure that the power alarm is properly armed, the DET_RESET (SPI-3, register 1, B<20>) bit should be resent after the transmitter has been enabled. To do this, register 1 is written a second time.

POWER ALARM DETECTOR

The TRF2443 integrates power-alarm indicator circuitry that allows monitoring of the TX output power and issuing an alarm (PWRDET pin LOW) if the output power goes below a threshold level.

The power-alarm indicator includes a peak detector, a comparator with a programmable threshold level, and power-alarm logic (see Figure 105).

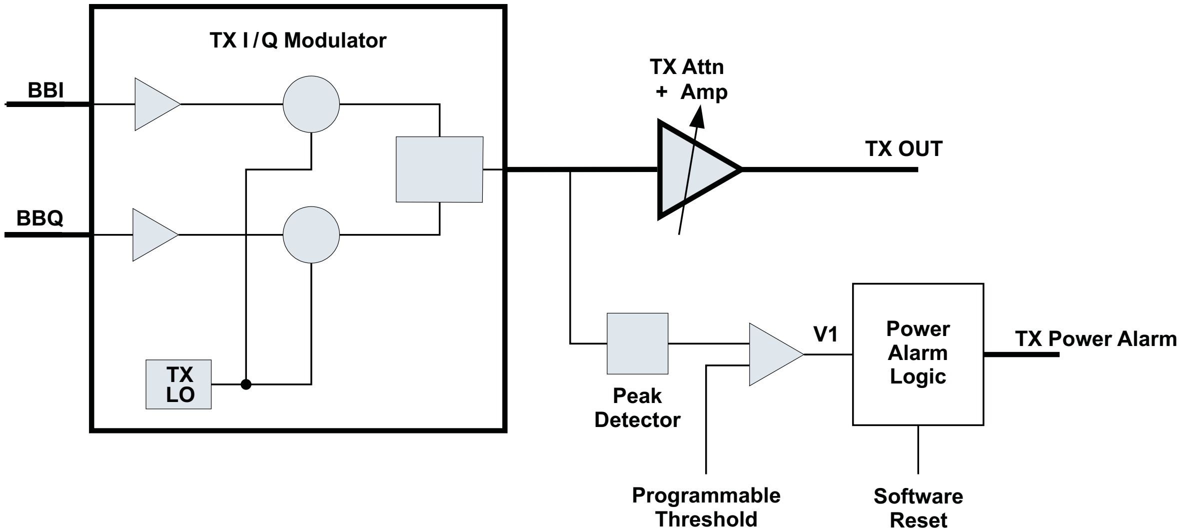


Figure 105. Block Diagram of the TX Power-Alarm Implementation

The peak detector measures the signal power level at the modulator output and provides a dc level proportional to the measured level. The peak-detector output is compared to a programmable reference threshold and the comparator output (V1) goes HIGH if the measured level is below the threshold level (see Figure 106).

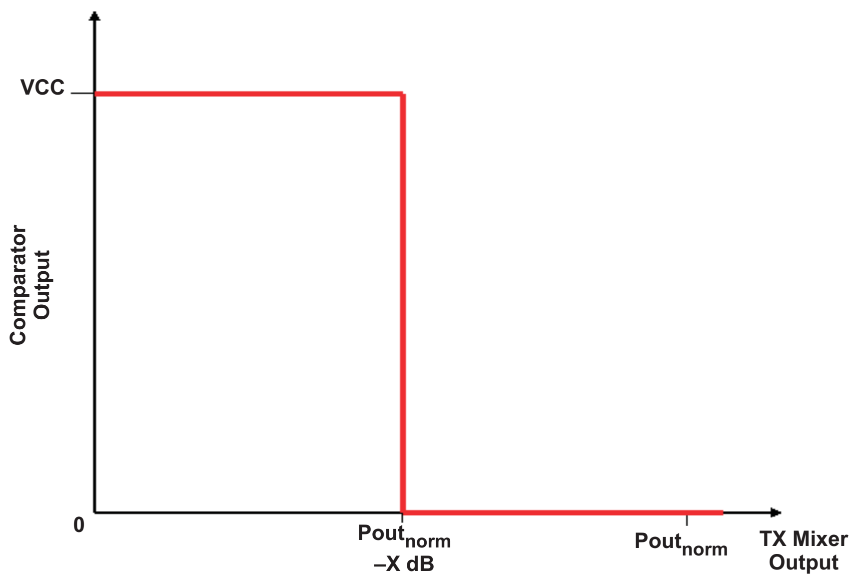


Figure 106. Expected Output of the Comparator

The power-alarm logic includes a time counter which is used to measure how long the IQ modulator output power stays below the user-specified threshold level. The counter is enabled when the comparator output (V1) is HIGH and the PWRDET pin is HIGH, but it is reset to 0 when the comparator output is LOW. If the time counter reaches the target count and V1 is still HIGH (that is, the IQ modulator output power is still low), then the logic goes in power-alert mode and PWRDET pin goes LOW. The power-alarm logic stays in the power-alert mode until a software reset is programmed. The device recognizes a software reset as a transition from 0 to 1 of the controlling bit DET_RESET (SPI-3, register 1, B<20>). Figure 107 illustrates how the power-alarm logic works from power up of the IC.

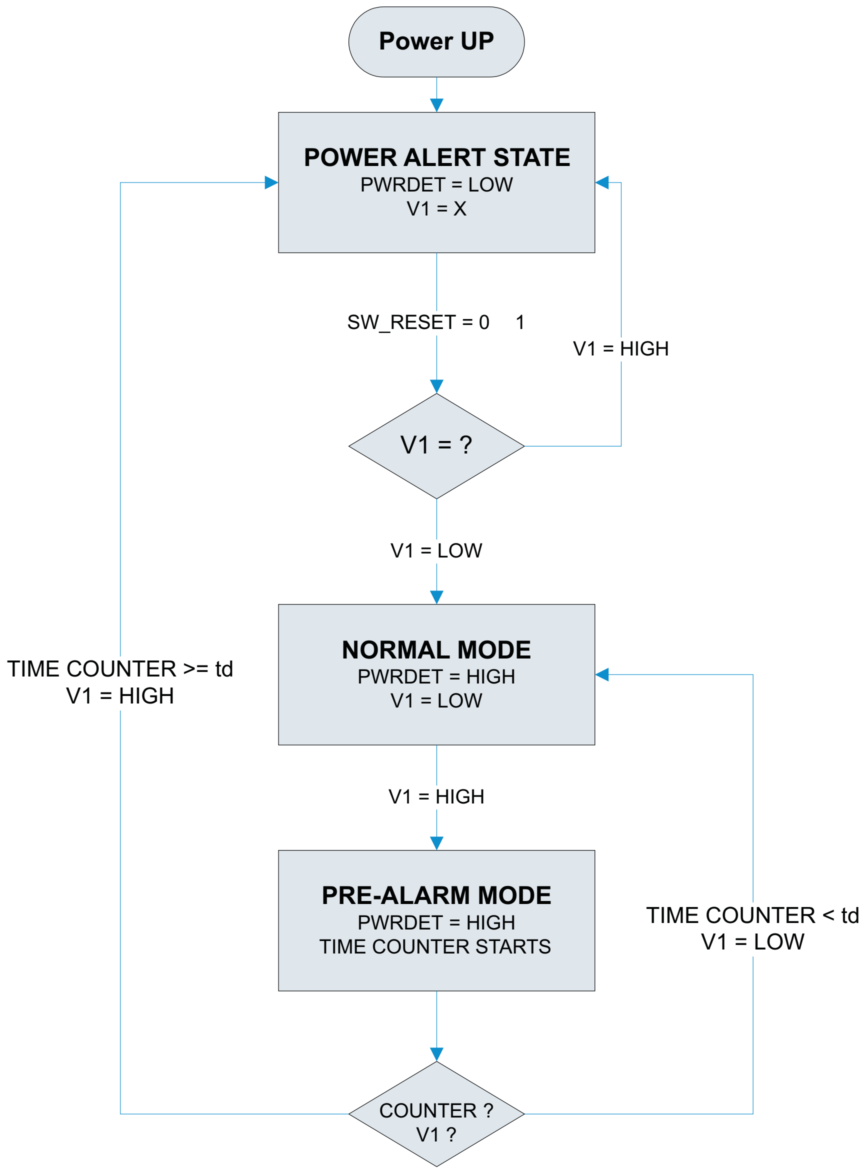


Figure 107. TX Power-Alarm Flow Chart

TX OUTPUT POWER RAMP-DOWN

To avoid unwanted spurious emissions during power down of the transmitter, the power-down circuitry is designed to ramp down the output power gradually. The ramp-down time constant is programmable. PS_TC<1,0> (SPI-3, register 3, B<10,9>) allows selection of four different time constants.

PS_TC	POWER DOWN
00	28 μs
01	42 μs
10	57 μs
11	75 μs

The values shown in the preceding table are the typical times required for the output level to be attenuated by 30 dB.

LOOPBACK

The TRF2443 integrates a loopback switch between the TX and the RX chains. The switch connects the TX modulator output to the RX IFVGA3 input. This path can be used for three different functions:

- Loopback path for the transmitted signal
- RX baseband low-pass-filter corner-frequency calibration
- TX modulator LO leakage calibration

The loopback mode is enabled by setting EN_LB (SPI-3, register 1, B<18>) to 1. When the switch is activated, the TX amplifier, RX LNA, RX IFVGA1, and RX IFVGA2 are all turned off automatically.

The loopback path can be programmed with two different insertion losses:

- 20-dB insertion loss for the loopback path of the transmitted signal
- Minimum insertion loss for calibration mode

The attenuation mode is selected via EN_LB_ATT (SPI-3, register 1, B<19>).

EN_LB_ATT = 1 → 20-dB attenuation

EN_LB_ATT = 0 → minimum insertion loss

TX Signal Loopback

The TRF2443 internal feedback path can be used to loop back the TX signal(1), which enables the RX chain to be used to monitor the transmitted signal. This mode is controlled via the serial programming interface (SPI) according the following possible steps:

1. Enable loopback switch with 20-dB attenuation
   a. EN_LB_ATT = 1 (SPI-3, register 1, B<19>)
   b. EN_LB = 1 (SPI-3, register 1, B<18>)
2. Program TXLO to 165 MHz (TXLO to 2640 MHz and TX divider to 16)
   a. TXRDIV<13,0> = <00 0000 0000 0001> (SPI-1, register 1, B<18,5>) [R = 1]
   b. TX_NINT<15,0> = <0000 0000 0100 0010> (SPI-1, register 2, B<20,5>) [N = 66]
   c. TXDIV_SEL = 0 (SPI-1, register 2, B<26>) [LO divider set to 16]
3. Program RXLO to 165 MHz (RXLO to 2640 MHz and RX divider to 16)
   a. RXRDIV<13,0> = <00 0000 0000 0001> (SPI-2, register 1, B<18,5>) [R = 1]
   b. RX_NINT<15,0> = <0000 0000 1000 0100> (SPI-2, register 2, B<20,5>) [N = 132]
   c. RXDIV_SEL = 0 (SPI-2, register 2, B<26>) [LO divider set to 16]
4. Set receiver baseband gain to 10 dB
   a. RXBB_GAIN<4,0> = <00001> (SPI-3, register 2, B<15,11>)
5. Program the receiver baseband-filter cutoff frequency to the appropriate value (depending on the TX signal bandwidth).

(1) For a TX loopback frequency of 165 MHz, the PLLs are locked to a 20-MHz PFD frequency.

Baseband-Filter Cutoff-Frequency Calibration

The TRF2443 internal feedback path can be used to set up an automatic calibration of the RX baseband-filter cutoff frequency. The procedure to calibrate the corner frequency to 3 MHz is described as follows.

1. Enable loopback switch with minimum insertion loss.
   a. EN_LB_ATT = 0 (SPI-3, register 1, B<19>)
   b. EN_LB = 1 (SPI-3, register 1, B<18>)
2. Program RXLO to 165 MHz (RXLO to 2640 MHz and RX divider to 16).
   a. RXRDIV<13,0> = <00 0000 0000 0001> (SPI-2, register 1, B<18,5>) [R = 1]
   b. RX_NINT<15,0> = <0000 0000 1000 0100> (SPI-2, register 2, B<20,5>) [N = 132]
   c. RXDIV_SEL = 0 (SPI-2, register 2, B<26>) [LO divider set to 16]
3. Set TXVCO divider to 16.
   a. TXDIV_SEL = 0 (SPI-1, register 2, B<26>) [LO divider set to 16]
4. Set the TXPLL PFD frequency to 4 MHz (R divider = 5).
   a. TXRDIV<13,0> = <00 0000 0000 0101> (SPI-1, register 1, B<18,5>) [R = 5]
5. Apply a dc offset at the TRF2443 TX baseband inputs (to increase the TXLO leakage at the modulator output).
6. Set the RX baseband amplifier gain to 22 dB.
   a. RXBB_GAIN<4,0> = <01101> (SPI-3, register 2, B<15,11>)
7. Set the RX baseband cutoff-frequency bit controls RXBB_FREQ<6,0> = 011 1000 (typical value for f_C = 3 MHz)
8. Program the TXLO frequency to 166 MHz (TXVCO = 2656 MHz).
   a. TX_NINT<15,0> = <0000 0001 0100 1100> (SPI-1, register 2, B<20,5>) [N = 332]
9. Measure the RX baseband output-power level (at I or Q output): Pout1.
10. Program the TXLO frequency to 168 MHz (TXVCO = 2688 MHz).
   a. TX_NINT<15,0> = <0000 0001 0101 0000> (SPI-1, register 2, B<20,5>) [N = 336]
11. Measure the RX baseband output power level (Pout2) and calculate attenuation: Att = Pout1 – Pout2.
12. If Att < 3 dB, then increase RXBB_FREQ and go back to 11); else if Att > 3 dB, then reduce RXBB_FREQ and go back to 11). This is repeated until two sequential iterations result in the calculated attenuation being above and below 3 dB. When this is observed, save the RXBB_FREQ value which results in an attenuation value closer to 3 dB.

The TRF2443 baseband low-pass filter cutoff frequency can be programmed to any of 128 cutoff frequencies. The cutoff frequency control consists of 7 bits, RXBB_FREQ<6,0>, which are located in SPI-3, register 2, B<22,16>. RXBB_FREQ<6,0> = <111 1111> corresponds to the minimum corner frequency. Figure 108 shows the 3-dB bandwidth of the filter versus all possible SPI codes for a typical unit. Figure 109 shows the inverse of the 3-dB bandwidth versus all possible SPI codes for a typical unit.

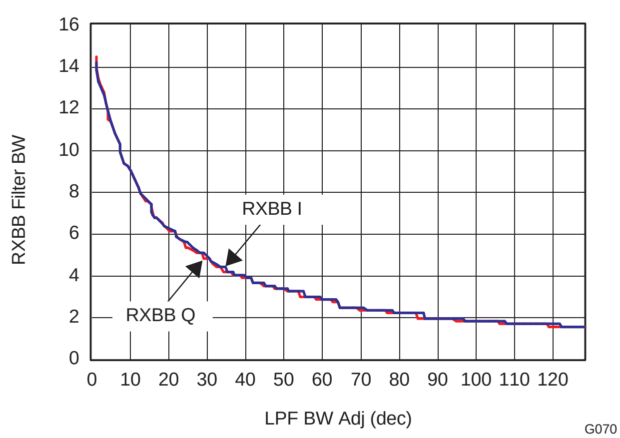


Figure 108. BW vs SPI Code (RXBB_FREQ<6,0>

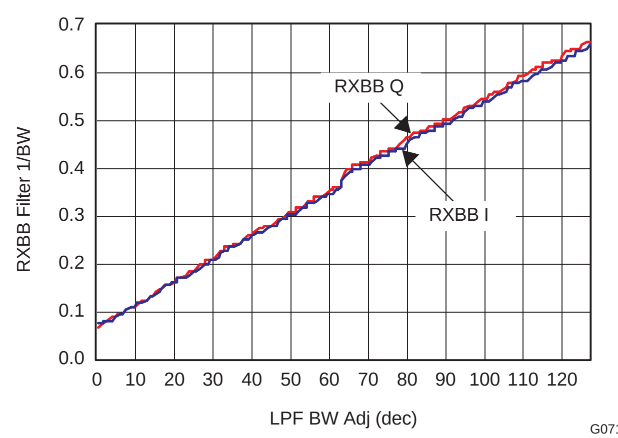


Figure 109. 1/BW vs SPI Code (RXBB_FREQ<6,0>

Because the corner frequency is dependent on the on-chip capacitance, it is possible to observe variations from unit to unit in the SPI code that yields a fixed corner frequency. Variations in capacitance from unit to unit result in a unique 1/BW curve for each unit. If the same DUT is to be used at multiple corner frequencies, the user should calibrate the DUT as described above to determine, at a minimum, 2 points on the 1/BW curve. From these calibrated points, any other corner frequency can be extrapolated using linear regression.

TX LO Leakage Calibration

The TRF2443 internal feedback path can be used to set up an automatic calibration of the TX LO leakage according the following potential procedure:

1. Enable loopback switch with minimum insertion loss.
   a. EN_LB_ATT = 0 (SPI-3, register 1, B<19>)
   b. EN_LB = 1 (SPI-3, register 1, B<18>)
2. Set RXLO = 330 MHz (RXVCO to 2640 MHz and RX divider to 8)
   a. RXRDIV<13,0> = <00 0000 0000 0001> (SPI-2, register 1, B<18,5>) [R = 1]
   b. RX_NINT<15,0> = <0000 0000 1000 0100> (SPI-2, register 2, B<20,5>) [N = 132]
   c. RXDIV_SEL = 1 (SPI-2, register 2, B<26>) [LO divider set to 8]
3. Set RX baseband in filter bypass mode and gain = 22 dB
   a. RXBB_GAIN<4,0> = <01101> (SPI-3, register 2, B<15,11>) [gain = 22 dB]
   b. RXBB_FLT_BYP = 1 (SPI-3, register 2, B<23>) [bypass filter]
4. Program TX LO in normal mode (TXLO = 340 MHz).
   a. TXRDIV<13,0> = <00 0000 0000 0001> (SPI-1, register 1, B<18,5>) [R = 1]
   b. TX_NINT<15,0> = <0000 0000 0100 0100> (SPI-1, register 2, B<20,5>) [N = 68]
   c. TXDIV_SEL = 1 (SPI-1, register 2, B<26>) [LO divider set to 8]
5. Measure power level at RXBB output at 10 MHz = P1.
6. Change TX input dc offset until minimum P1 is achieved.

The TRF2443 TX baseband inputs can be ac- or dc-coupled to the external digital-to-analog converter (DAC). In case of direct coupling, the DAC must provide the appropriate dc offset of step 6 to null the LO leakage. If an ac-coupled approach is selected, then the internal bias must be enabled by setting EN_TXCM = 1 (SPI-3, register 3, B<31>). In this case, the integrated dc DAC controls the baseband dc offset. The internal DAC is programmed via the SPI. TXBBI<5,0> (SPI-3, register 3, B<30,25>) and TXBBQ<5,0> (SPI-3, register 3, B<24,19>) control the internal DAC settings.

TXBBI<5,0> = TXBBQ<5,0> = <10 0000> corresponds to midrange, that is, no offset applied.

RX IMAGE REJECTION

The TRF2443 has been designed to provide optimal image rejection. Using symmetry in the design of the I and Q paths of the receiver ensures that mismatch between the I and Q paths is minimized. Image rejection is a function of the amplitude (A) mismatch and the phase error (Φ) from 90 degrees of the I and Q RX baseband signals. Image rejection is calculated in the following manner:

$$\text{Rejection(dB)} = 10\log\left[\frac{A^2 - 2A\cos\phi + 1}{A^2 + 2A\cos\phi + 1}\right]$$

DC-OFFSET CALIBRATION

The TRF2443 provides an automatic calibration procedure for adjusting the dc offset in the receiver and XPIC baseband I/Q paths. The internal calibration requires a clock in order to function. This clock is derived internally from the reference clock with a frequency divider, whose divider ratio is programmable. DCOFF_CLK<2,0> (SPI-3, register 5, B<16,14>) and XDCOFF_CLK<2,0> (SPI-3, register 5, B<29,27>) set the division ratio for the dc-offset correction-loop clock for the receiver and XPIC chains, respectively.

The output full-scale range of the internal dc-offset-correction DAC is programmable using bits DCOFF_BIAS<1,0> (SPI-3, register 5, B<13,12>) for the receiver chain and XPICDCOFF_BIAS<1,0> (SPI-3, register 5, B<26,25>) for the XPIC chain. The range is shown in Table 11.

Table 11. DC Offset Correction DAC Programmable Range

DCOFF_BIAS _B1 XPICDCOFF_BIAS _B1	DCOFF_BIAS _B0 XPICDCOFF_BIAS _B0	FULL SCALE
0	0	10 mV
0	1	20 mV
1	0	30 mV
1	1	40 mV

The I- and Q-channel output maximum dc-offset correction range can be calculated by multiplying the values in Table 11 by the baseband PGA gain. The LSB of the digital correction is dependent on the programmed maximum correction range. The dc offset correction DAC output is affected by a change in the PGA gain, but if the initial calibration yields optimum results, then the adjustment of the PGA gain during normal operation does not significantly impair the dc offset balance.

The dc offset correction DACs are programmed from the internal registers when the RXBB_CALSELECT bit (SPI-3, register 7, B<21>) is set to 1 (default value at power on). At start-up, the internal registers are loaded at half-scale, corresponding to a decimal value of 128. The autocalibration for the receiver chain is initiated by setting the EN_BB_AUTOCAL bit (SPI-3, register 5, B<5>) to 1. When the calibration is over, this bit is automatically reset to 0. Similarly for the XPIC, by programming EN_XPIC_AUTOCAL (SPI-3, register 5, B<18>) to 1, the baseband dc-offset calibration starts. During calibration, the RX local oscillator must be on. At each clock cycle during an autocalibration sequence, the internal circuitry senses the output dc offset and calculates the new dc current for the DAC. After the 13th clock cycle, the calibration is complete and the EN_BB_AUTOCAL (or EN_XPIC_AUTOCAL) bit is reset to 0. The dc-offset DAC state is stored in the internal registers and maintained as long as the power supply is kept on or until a new calibration is started.

The required clock speed for the optimum calibration is determined by the internal detector behavior (integration bandwidth, gain, sensitivity). The speed of the clock can be slowed down by selecting a clock divider ratio DCOFF_CLK<2,0> (SPI-3, register 5, B<16,14>) and/or XDCOFF_CLK<2.0> (SPI-3, register 5, B<29,27>). The detector has more averaging time the slower the clock; hence, it can be desirable to slow down the clock speed for a given condition to achieve optimum results.

The internal registers controlling the internal dc current DAC for the receiver chain are accessible through the SPI (SPI-3, register 7, B<20,5>), providing a user-programmable method for implementing the dc-offset calibration. To employ this option, the RXBB_CALSELECT (SPI-3, register 7, B<21>) bit must be set to 0. During this calibration, an external instrument monitors the output dc offset between the I/Q differential outputs and programs the internal registers RXBBI_DCOFF<7,0> (SPI-3, register 7, B<12,5) and RXBBQ_DCOFF<7,0>, (SPI-3, register 7, B<20,13) to cancel the dc offset.

TEMPERATURE SENSOR

The TRF2443 integrates a temperature sensor that can be used to monitor the die junction temperature. To enable it, PWD_TEMPSENS (SPI-3, register 4, B<22>) must be set to 0. The temperature sensor generates a dc voltage proportional to the measured temperature. This voltage is output at the TEMPOUT pin (pin 37). The output voltage goes typically from 500 mV at –40°C to 970 mV at 150°C.

The temperature sensor output can also be read through the SPI. An internal ADC converts the analog information to digital bits. The internal data-converter is enabled by setting PWD_TEMPADC (SPI-3, register 4, B<21>) to 0. The conversion starts when ADC_START (SPI-3, register 4, B<5>) is set to 1. The internal ADC uses a clock (ADC clock) generated from the external reference clock with a divide-by-16 frequency divider. At the end of conversion, ADC_START is reset to 0 and the 8-bit word ADC output is transferred into SPI-3, register 0, B<29,22>, where it can be read through the readback mode (See the *READBACK MODE* section). When the data conversion from analog to digital is complete, the CONVDONE bit (SPI-3, register 0, B<5>) is set to 1. If the ADC input signal is outside its input voltage range, the OUTRANGE bit (SPI-3, register 0, B<6>) is 1. The ADC input voltage range is 1 V, from 0.125 V to 1.125 V.

APPLICATION SCHEMATIC

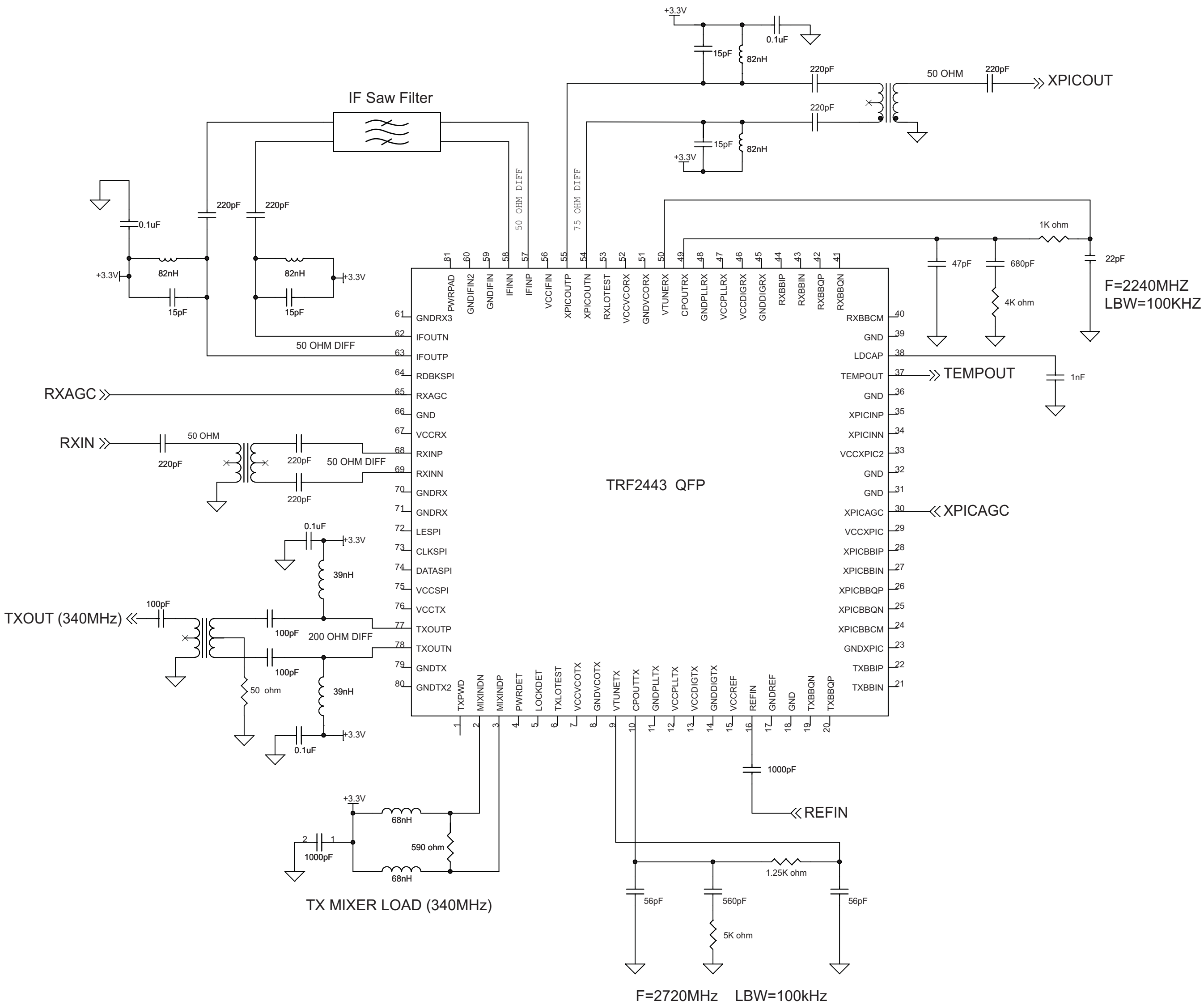


Figure 110. TRF2443 Application Schematic

Table 12. Pin Termination Requirements/Limitations

NAME	PIN	DESCRIPTION
IFOUTN/IFOUTP	62, 63	IFVGA1 open-collector output terminals. A pullup inductor from each pin to the power supply is required.
GND	18	Ground pin shorted to package thermal pad. To be connected to the same ground plane as GNDREFIN (pin 17).
IFINP/IFINN	57, 58	IFVGA2 differential input pins internally matched to 50 Ω.
LDCAP	38	Lock-detector capacitor pin. The size of capacitor on this pin sets the time constant of the lock-detect circuit. Suggested value for 20-MHz PFD frequency: connect a 1-nF capacitor to ground on this pin (10-µs deglitch time).
MIXINDN/ MIXINDP	2, 3	TX IQ modulator open-collector load terminals. A pullup inductor from each pin to the power supply is required. A shunt load resistor is required.
PWRDET, LOCKDET, RDBKSPI	4, 5, 64	TRF2443 digital output pins can sink/source up to 8 mA of current.
REFIN	16	PLL reference clock input. External ac-coupling capacitor required, as pin is internally dc-coupled.

Table 12. Pin Termination Requirements/Limitations (continued)

NAME	PIN	DESCRIPTION
RXAGC	65	Receiver-chain VGA gain-control dc-voltage input. Equivalent input impedance: 100 kΩ in series with 4 pF.
RXINP/ RXINN	68, 69	RX input differential terminals. Input impedance is 50 Ω differential. A 1:1 balun is required to drive it single-ended.
RXLOTEST	53	RX VCO output pin: test output to check internal RX local oscillator. If it is not used, the pin can be grounded.
TEMPOUT	37	Temperature-sensor output. If temperature sensor is not used (disabled), this pin should be terminated with a 100-kΩ resistor to ground. If it used, the TEMPOUT buffer can drive impedances of R > 10 kΩ and C < 100 pF.
TXLOTEST	6	TX VCO output pin: test output to check internal TX local oscillator. If it is not used, the pin can be grounded.
TXBBIP/ TXBBIN	22, 21	TX baseband I-channel differential inputs. If EN_TXCM (SPI-3, register 3, B<31>) = 0, external AC coupling caps and 100-Ω differential resistor is required.
TXBBQP/ TXBBQN	20, 19	TX baseband Q-channel differential inputs. If EN_TXCM (SPI-3, register 3, B<31>) = 0, external AC coupling caps and 100-Ω differential resistor is required.
TXOUTP/ TXOUTN	77, 78	TX amplifier open-collector output terminals. A pullup inductor from each pin to power supply is required. Output impedance is set typically to 200 Ω differential. A 4:1 impedance-ratio balun is needed to transform to 50 Ω single-ended.
TXPWD	1	TX power down; digital input
VCCRX	67	RX-chain power supply. The decoupling capacitor on this power supply should be connected to the same ground plane to which the GNDRX pins, 70 and 71, are connected.
XPICAGC	30	XPIC chain VGA gain-control dc-voltage input. Equivalent input impedance: 100 kΩ in series with 4 pF.
XPICOUTN/ XPICOUTP	54, 55	XPIC output-amplifier open-collector output terminals. Output impedance is set typically to 75 Ω differential with an internal resistor so that no external load is required. A pullup inductor from each pin to the power supply is required. A 1:1 impedance ratio balun is needed to transform to 75 Ω single-ended.

EVM BOARD LAYOUT

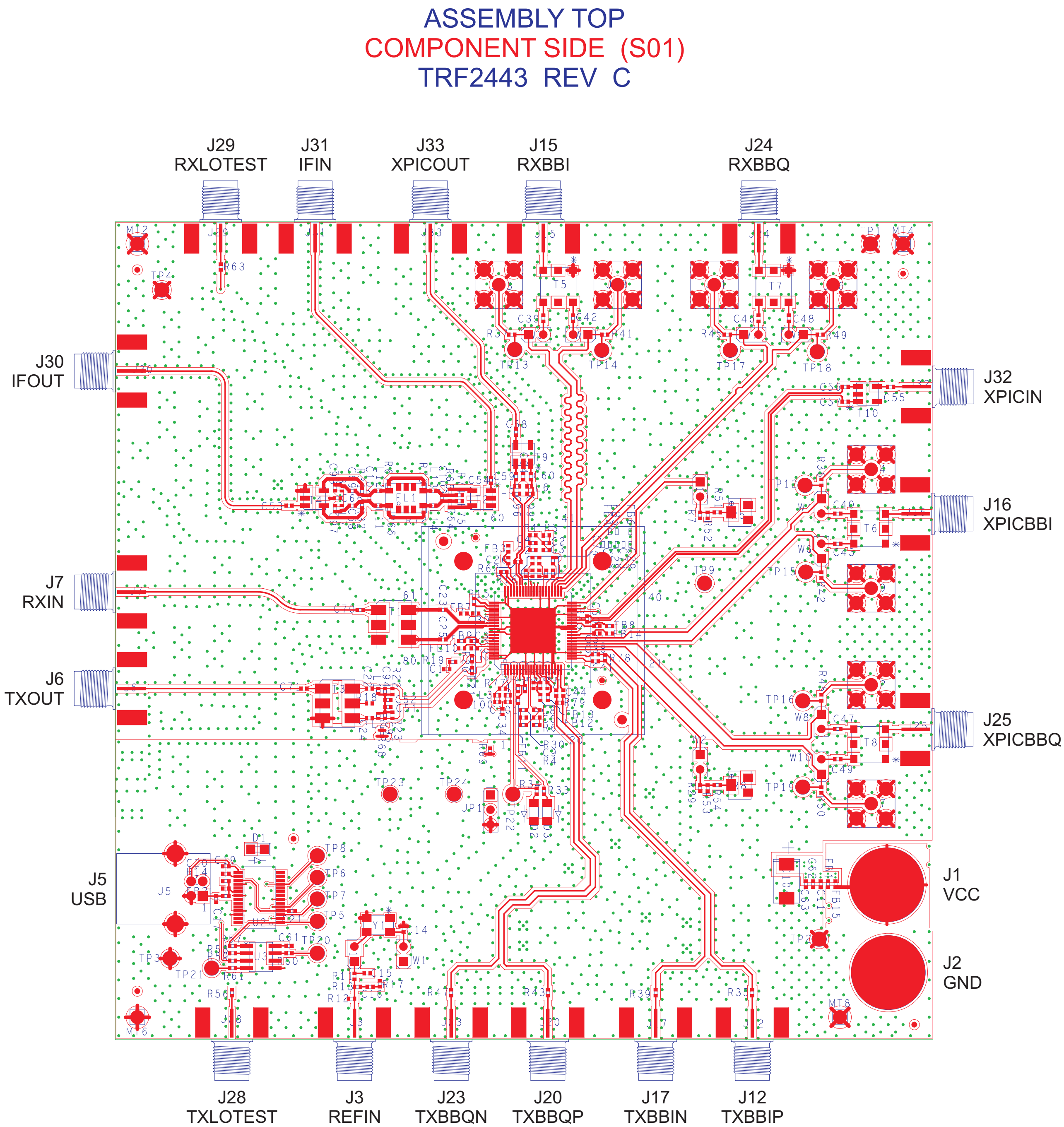


Figure 111. TRF2443 EVM Top Layer

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TRF2443IPFP	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TRF2443IPFPR	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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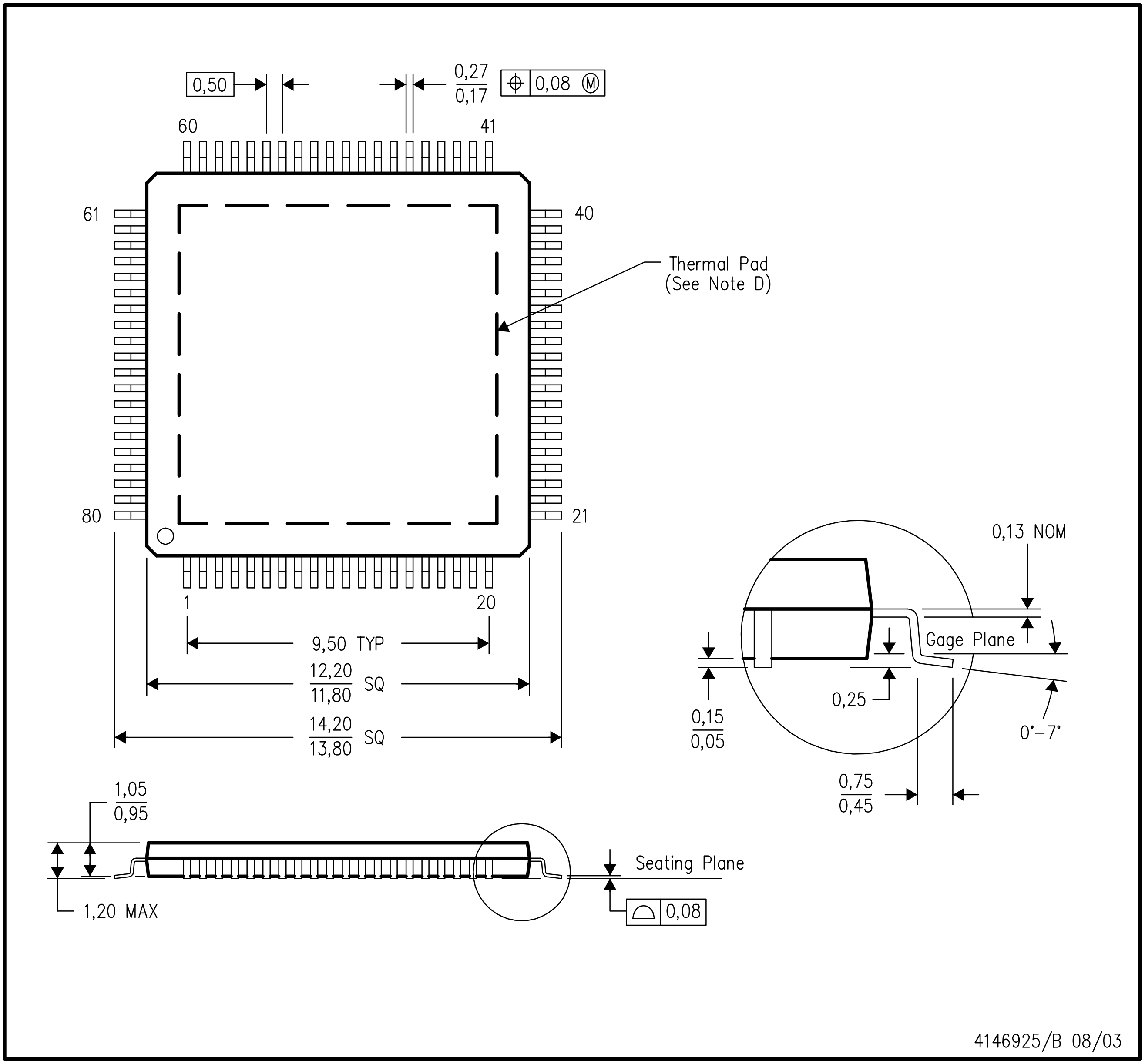
PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. Falls within JEDEC MS-026

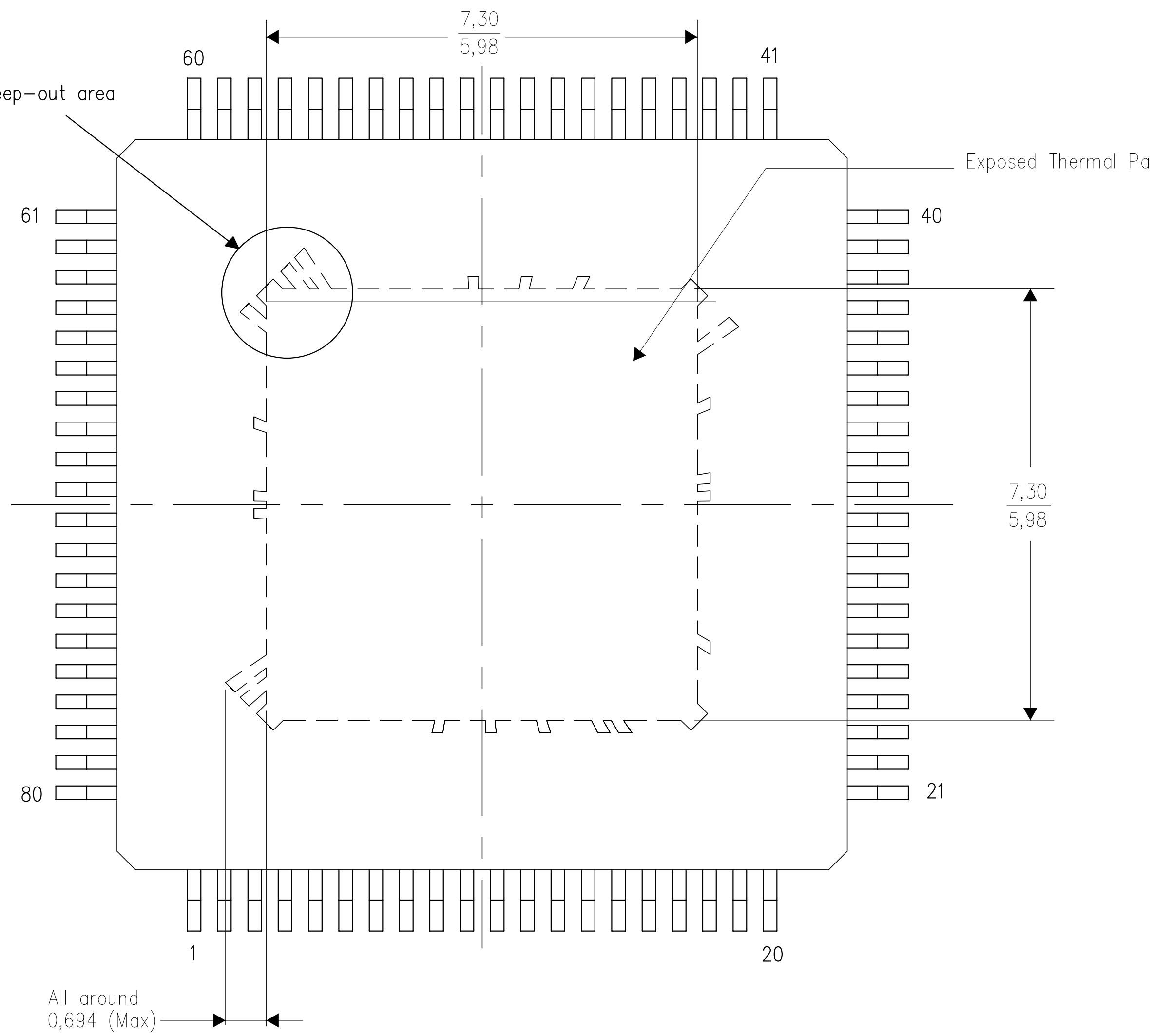
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions 4206327-5/K 06/10